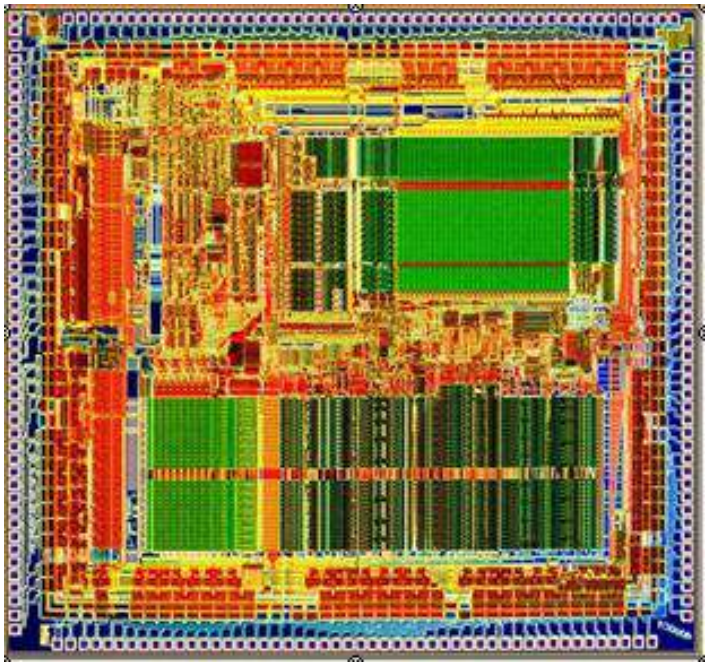
LAKSHMI NARAIN COLLEGE OF TECHNOLOGY EXCELLENCE

LNCT GROUP OF COLLEGES "WORKING TOWARDS BEING THE BEST"

VLSI Design
[EC-701]
Laboratory Manual



Submitted by: **Submitted To:**

Enrollment No:

Department of Electronics & Communication Engineering

VISION OF THE DEPARTMENT

To become reputed in providing technical education in the field of electronics and communication engineering and produce technocrats working as leaders.

MISSION OF THE DEPARTMENT

1. ***To provide congenial academic environment and adopting innovative learning process.***

2. ***To keep valuing human values and transparency while nurturing the young engineers.***

3. ***To strengthen the department by collaborating with industry and research organization of repute.***

4. ***To facilitate the students to work in interdisciplinary environment and enhance their skills for employability and entrepreneurship.***

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

PEO1: Recognize and apply appropriate experimental and scientific skills to solve real world problems to create innovative products and systems in the field of electronics and communication engineering.

PEO2: To evolve graduates with ability to apply, analyze, design in Electronics & Communication Systems.

PEO3: Motivate graduates to become responsible citizens with moral & ethical values for the welfare of Society.

PEO4: Inculcate the habit of team work with professional quality of leadership to become successful contributors in industry and/ or entrepreneurship in view of Global & National status of technology.

PROGRAM SPECIFIC OUTCOME (PSO)

PSO1: Analyze specific engineering problems relevant to Electronics & Communication Engineering by applying the knowledge of basic sciences, engineering mathematics and engineering fundamentals.

PSO2: Apply and transfer interdisciplinary systems and engineering approaches to the various areas, like Communications, Signal processing, VLSI and Embedded system, PCB Designing.

PSO3: Inculcate the knowledge of Engineering and Management principles to meet demands of industry and provide solutions to the current real time problems.

PSO4: Demonstrate the leadership qualities and strive for the betterment of organization, environment and society.

General Lab Policies

- All labs must be attended and completed. In the event that you cannot attend a lab, prior approval must be obtained. In such case, it is required that you make up the lab at another time.

- Satisfactory completion of all the labs is required for passing the course. If you are unable to complete the lab in the assigned lab time, it is expected that you would complete the lab on your own.

- At the beginning of a lab session, the instructor will collect report for the previous week's lab. Any late lab report will have its grade reduced. If, for any valid reason, you are not able to meet the deadline, let the instructor know well in advance of start of the lab.

- You are responsible for keeping track of your e-mail. In case of difficulty with any specific lab or any other problem concerning the lab, please come and talk to the lab instructor or use e-mail.

Student Name

Signature _____

Instructor Name

Signature _____

Lab Report Instructions

The lab report should be brief and have the following sections:

- Cover page: Name(s), section, and lab.
- Contents / Index
- Introduction: A small paragraph describing the intent of the lab. This should NOT be a rephrasing of the lab objective in the lab handout but a description from the student's own experience.
- Results and Answers to Questions: This section should discuss the lab results (if any) and would answer the questions at the end of the lab handout (if any). Compare the simulations results with hand calculations and comment on any discrepancies if any.
- Lessons learned: Share the lessons learned from the lab. This includes anything related to circuits, Electric CAD, Spice modelling etc. You are also encouraged to include any suggestions for improving the lab handout.
- Attachments: All attachments must have a clear title and page number for cross referencing. Include only the results that support you discussion earlier in the report.
- The lab reports must be typed and should be the student's original work. Do not copy and paste material from the lab handouts to your lab report. If you use any material by another author (a paper, a book etc.), give proper credit to the original author. Not only is this professional courtesy to do so but is required of you in order to avoid any appearances and occurrences of plagiarism.

Lakshmi Narain College of Technology Excellence, Bhopal

Department of Electronics & Communication Engineering

EC-701
VLSI Design LAB
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Lakshmi Narain College of Technology Excellence, Bhopal
Department of Electronics & Communication Engineering
Experiment -1

Study of VLSI Design methodologies and limitations using CAD tools for CMOS technology

Aim / Objective : Study of VLSI Design methodologies and limitations using CAD tools for CMOS technology. (a) VLSI Technology and Design

(b) Custom v/s Semi Custom Design

(c) Design Complexities

(d) CAD for VLSI

(e) VLSI CAD classification

(f) Design Flows **Study Details:**

To study various VLSI design methodologies in VLSI Design. Various technology and associated design constraints will also be studied. A brief comparison is also studied between semi custom and custom design. A sideways study is also performed on design complexities and CAD for VLSI.

Introduction:

As CMOS Technology is growing at a rapid rate, analogous developments can be seen in every peripheral domain, especially CAD tools. In large design projects, it is desirable to compare different hierarchical models at various levels of design abstraction with respect to existing technologies. The selection of the available technology, circuit and system parameters also do depend on the application being implemented along with the availability of CAD tools. VLSI CAD tools have emerged as a boon in assisting VLSI Design engineers to choose and optimize various design models and technology. The importance of CAD tool can be understood by seeing its complex algorithms, data structures and modeling assumptions used in each of the following steps namely logic synthesis, logic verification, layout synthesis and timing verification. VLSI CAD flow mainly break the design problem into smaller steps, each step renders design a little more reality. The synthesis and verification steps make us look forward and backward in design. The complete set of above steps is called a Flow.

An analysis of commercial VLSI Chips shows the integration density, computed with normalization, decreased significantly over the last couple of decades. Design automation is the main cause of this degradation. The importance of a well defined design methodology is often underestimated. In this lab report design methodologies and CMOS technology using CAD tools for complex VLSI chips will be discussed It will be stressed that the suppression of abstraction levels in a design methodology will lead to conceptually simple methodologies .As a result, the corresponding CAD tools will be more efficient.

VLSI Technology and Design

With the advent of Very Large Scale Integration (VLSI), rapid advances took place in circuit integration technologies; the electronics industry has achieved a phenomenal growth over the last two decades. Various applications of VLSI CMOS circuits in highperformance computing, telecommunications, and consumer electronics has been expanding progressively, and at a very hasty pace. Steady advances in semi-conductor technology and in the integration level of Integrated circuits (ICs) have enhanced many features, increased the performance, improved reliability of electronic equipment, and at the same time reduce the cost, power consumption and the system size. With the increase in the size and the complexity of the analog and digital systems, Computer Aided Design (CAD) tools are introduced into the hardware design process. Design Methodologies are necessary for a systematic design. The chip design process enforced the automation of process, automation of simulation based verification i.e. replacing of traditional breadboard techniques through HDL (hardware description language) development. The various modular hierarchical techniques of design created the scenario that CAD tools are inevitable. A VLSI System integrates millions and millions of electronic components in a small area. The main objective is to make the analog or digital system as compact as possible with the required functionalities. Tens and thousands of transistors are fabricated on a small piece of wafer. The circuits are tested and fabricated because once an error is created the whole design is waste and it costs million and millions of dollars. Therefore CAD tools came into the picture. CAD tools are inevitable. This chip design forced

automation of process, automation of simulation based verification. This CAD assistance has lead to Electronic Design Automation.

Design Methods:

Systematic design methods or the design methodologies are necessary for successfully designing complex digital hardware. Our design methods usually differ by the number of abstraction levels and the complexities involved.

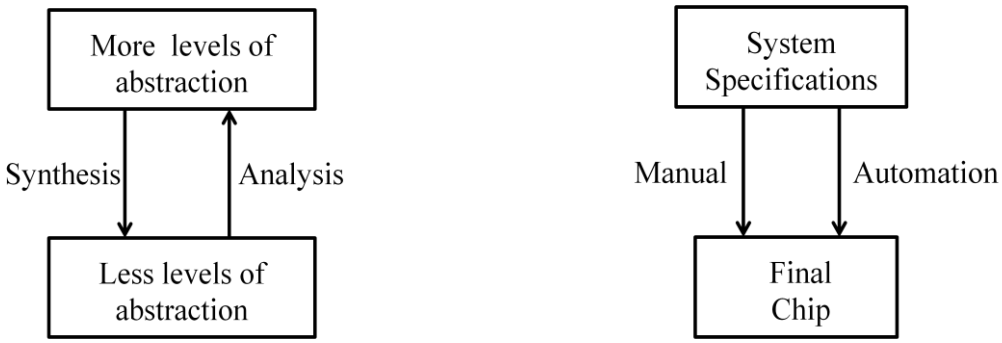


Fig 1. Abstraction Hierarchy

Comparing structurally different views of a VLSI Design include divide and conquer techniques which includes sorting by structure and sorting by issues.

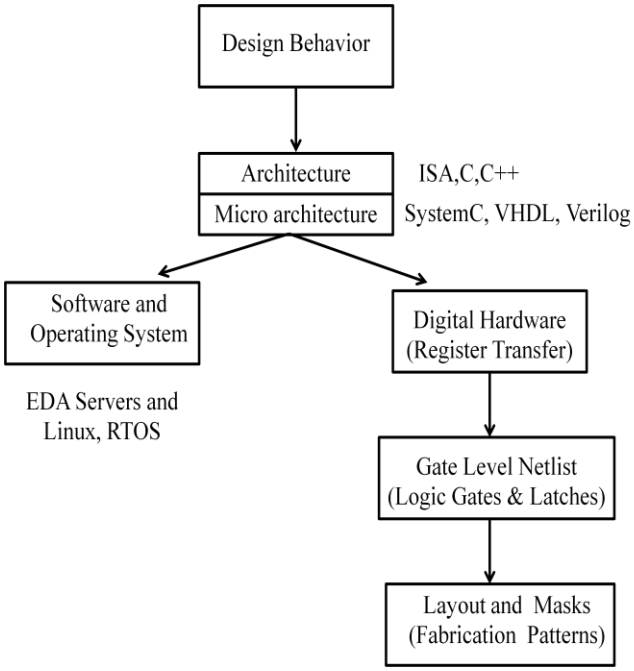


Fig 2 Design representation levels and formats associated

The design hierarchy that uses existing techniques has an unacceptable restriction that they use identical hierarchies. Structurally hierarchy transformation is the first step and hierarchy base comparison is the last step.

Complexities

A. Problem Domain Complexity

The functionality of the integrated chip should be taken into account with respect to the 3p's i.e. price, power and performance. The problem may be competing contradictory requirements in terms of speed power and other design metrics. The problem can also arise due to the mismatch between the users and designers. Application area specialization and knowledge with ever changing and evolving specifications. The cost of design and development also depends on the extent to which the specification issues have been captured.

B. Design/ Development Process Complexity

VLSI is a fast growing industry, if automobile industry would have developed at the same rate cars would have been far more affordable. The rapid change in technology is basically due to advancements in various fabrication procedures and simultaneously in design methodologies. The modularity and hierarchical let the large task into smaller modules, the large tasks requiring multidisciplinary team, separated by geographical regions.The design cycle may be short or can be long depends on the requirement of the requirement. Assuring integrity of the design and success requirement are the different parts in characterizing the design. Various methodologies look in to the design with multiple views and the representation will be different with each set of characterization.

The complexity can rise further due to insufficient documentation.

C. Complexity of choices

As the time goes on, advancement in the design methodologies have been done with respect to speed area and power dissipation. Many technologies and implementation choices such as NMOS, PMOS. Many methodologies (FPGA, Semi custom, CPLD, Full custom, ASIC etc.). Many different styles of implementation in static (ratioed, general transistor logic, pass transistor logic, transmission gate logic etc.). Many logic

styles in dynamic 2 phase,4 phase) Cascaded logic (Domino, NPMOS, Zipper etc.). Many possible partitions at each level increase the complexity of choices.

D. Complexities of design tasks

These complexities include various clocking and timing issues, testing related issues, packaging related issues and concurrency related operations. The design tasks exist in the front end as well as in the back end.

Computer Aided Design Technology for CMOS VLSI Design

As the manufacturing technology moves forward the ability to reap the full potential of available transistors and interconnect is increasingly important Design technology is concerned with the automated or semi automated conception, synthesis and verification and eventually testing of microelectronic systems. The design technology faces fundamental limitation in the computational intractability of the design optimizations.

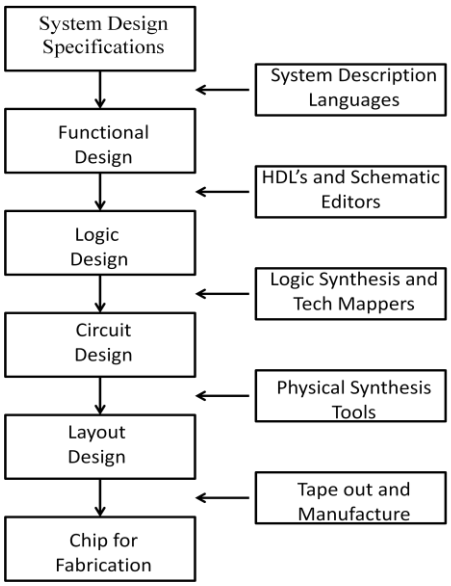


Fig. 3 Traditional VLSI Design Flow

The role of the CAD tool in VLSI design is

a) Accurately generated and easily modifiable graphical representation of the product. The user can nearly view the actual product on screen, make any modifications to it, and present his/her ideas on screen without any prototype, especially during the early stages of the design process.

b) Perform complex design analysis in short time and Implementing Finite Elements.

c) The user can perform the following analysis methods:
Static, Dynamic and Natural Frequency analysis, Heat transfer analysis, Plastic analysis, Fluid flow analysis, Motion analysis, Tolerance analysis, Design optimization.

d) Record and recall information with consistency and speed.

Co evolution of CAD Tools and Design Methodology with CMOS Technology

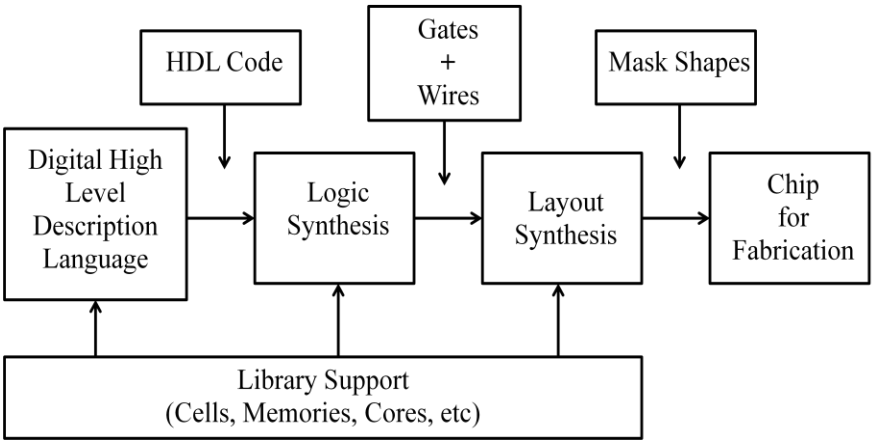


Fig.4 Co evolution of tools and methodology

The effectiveness of the design process is determined by its context, the design methodologies and flows we employ, and the designs that we essay by the perhaps more than by its component tools and algorithms.

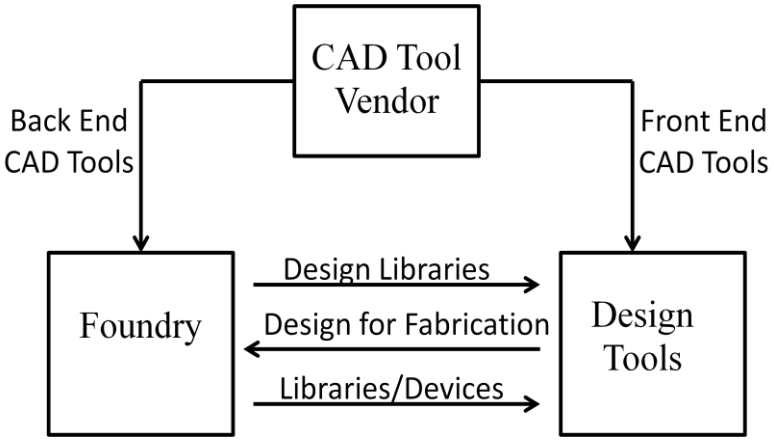


Fig.5 Co evolution of tools and methodology 2

VLSI CAD Tools

A kind of activity which uses a computer to assist on the creation, modification and analysis of design. CAD tools generally consist of the following components, input handler (input from mouse or keyboard), data structure and algorithms (in memory), output handler (output to display).

S.No.	CAD Tool	Open Source/ Licensed	Type	Function
1	Cadence EDA	Licensed	Analog and Mixed signal	Complete CAD Flow
2	Mentor Graphics EDA	Licensed	Analog and Mixed signal	Complete CAD Flow
3	Synopsys EDA	Licensed	Analog and Mixed signal	Complete CAD Flow
4	Tanner EDA	Licensed	Analog and Mixed signal	Complete CAD Flow
5	Alliance	Open Source	Mixed Signal	Logic to Layout
6	Electric CAD	Open Source	Mixed Signal	Logic to Layout
7	Magic	Open Source	Mixed Signal	Circuit Layout
8	SystemC	Open Source	Electronic System Level	Library for Digital Design

9	myHDL	Open Source	Electronic System Level	Hardware Description language

Fig. 6 Comparative study of various open source and licensed set of VLSI EDA tools.

The front end tools are used for design entry editors, simulation synthesis and timing analysis and test generation tools. The back end tools include floor planning place and route, extraction etc. Editors ,simulators, analyzers and synthesizers together contributes in computer oriented design.

VLSI CAD Tools Vs Methodology

As we make progress in design technology, there is a ongoing debate within the design technology community about the importance of new algorithms and tools or new methodologies and associated tool flows.The simple fact is that history of design for microelectronic systems includes the going of both of them hand in hand to get the maximum benefit and in act these two aspects of the design technology are tightly coupled and correlated in terms of their impact.

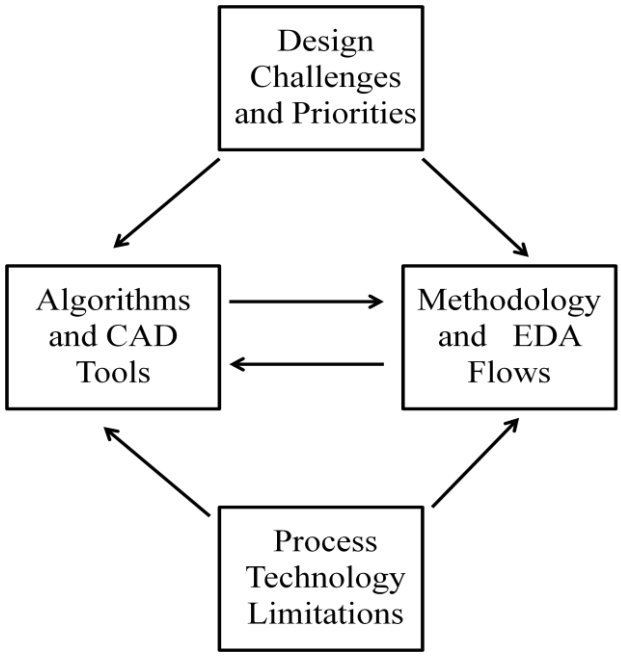


Fig.7 VLSI CAD/EDA vs CMOS Design Methodologies

VLSI Design incorporates both the design methodologies and associated CAD tools because both forms the integral parts and should go hand in hand as they evolve based on the designer's needs.

Limitations and Challenges to be overcome in CAD tools

In this section, various established and emerging design quality metrics and the main challenges of CAD tools to effectively predict, analyze their interactions, and optimize them in theCMOS technology were discussed. In the last few years, the research developers have witnessed increasing levels of interactions between physical, logical, and functional realms in the synthesis of VLSI circuit and systems. Various approaches with varying levels of interactions between the synthesis and layout phases have been proposed. These techniques are classified into several classes:

A. Gain-Based Synthesis: It is based on logical effort theory, which performs the gate sizing based on logical effort, electrical effort and timing constraints. The succeeding layout phase, is then performed with additional timing and capacitance constraints to meet the initial gate sizing decision. Appropriate circuit libraries are must.

B. Layout-Friendly Synthesis: Here, Synthesis of layout implications is given more importance. The wire planning is a best example for this type of synthesis. The research developers use the placement of I/O pins to achieve a layout-friendly logic factorization.

C. Layout-Driven Synthesis: In this synthesis depends on companion, layout/placement of various parts of the logic. After synthesis nodes may get created or deleted, and the companion layout may need to be updated to reflect these changes. The benefit of having a companion layout view is access to a more realistic estimates about the interconnect parasitic. This would allow the synthesis phase to make better decisions, while optimizing the logic.

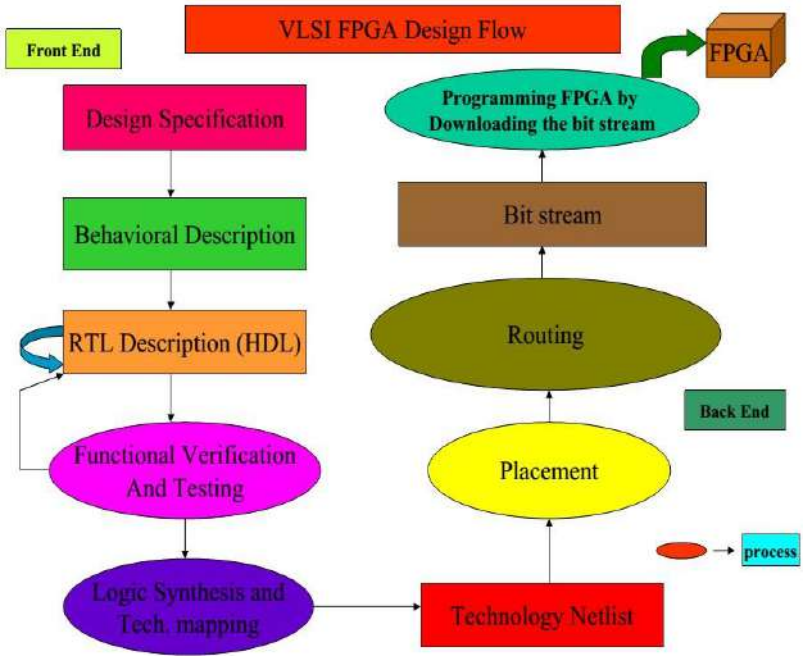
D. Integrated Synthesis and Layout: The ultimate integration of the synthesis and layout phases were carried out by this class.

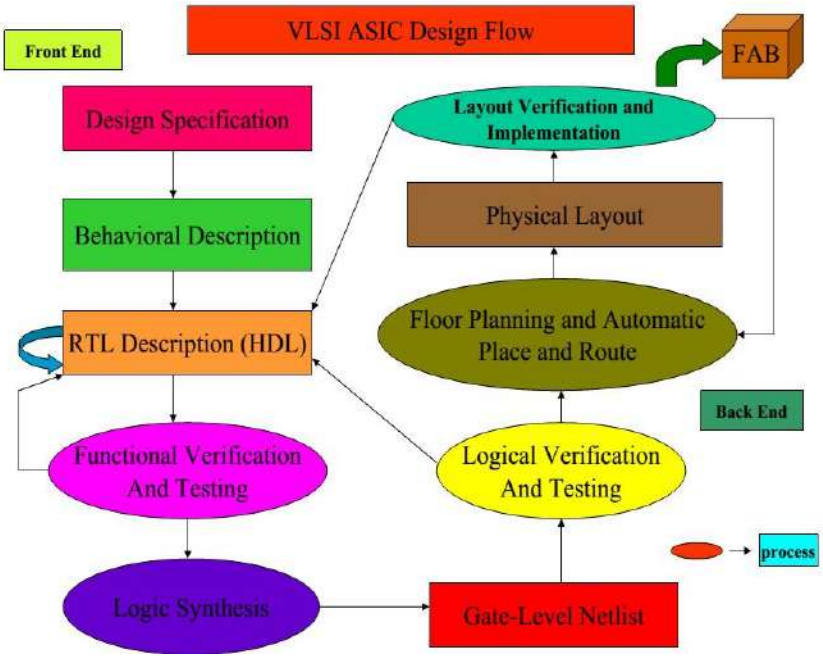
E. Synthesis-Driven Layout: This category consists of those techniques which perform layout optimization moves either within the synthesis phase or in a post-

layout phase where synthesis and layout optimizations are applied to improve the design or meet the performance constraints.

F. Synthesis-Friendly Layout: This type of synthesis consists of layout synthesis algorithms and environments which is capable of withstanding functional and logic changes, with minimal disruption to the layout.

Design Flows :





Summary:

With design technology, it would be possible to implement, verify and test the complex integrated circuits. It is through design technology that the ideas and objectives of design, circuit and fabrication engineers are transformed into reality and the quality of the design tools and associated methodologies determine the design time, performance, cost and the correctness of the final product chip. The development in the design tools, collaborative design methods, the role of human factors and integration factors in the design technology marks the outline of various design methodologies. This paper explains design quality metrics from a CAD tool perspective. Various shortcomings of the current CAD tools and methodologies to tackle the VLSI design challenges were discussed and several promising remedies and their implications on design and methodologies are explored.

Lakshmi Narain College of Technology, Bhopal
Department Of Electronics and Communication Engineering

Viva Questions

1. How is VLSI chip different from a PCB?
2. What are various VLSI Technology design Drivers?
3. What are the various VLSI Design Methodologies?
4. Explain VLSI Design flow?
5. What are various VLSI Design complexities?
6. Explain CAD for VLSI?
7. Give classification of VLSI CAD Tools?
8. Explain VLSI ASIC Design flow?
9. Explain VLSI FPGA Design flow?
10. What are the various limitations and challenges to be overcomed in VLS I design from an IC designer view?

Experiment -2

Using Electric CAD and SPICE simulation Software for VLSI

Aim/Objective :

Study, Installation and using CAD for VLSI Design

Design and Simulation of a resistive voltage divider and other circuits using LTSpice and Electric CAD and following operations for the same

(a) Operating point Analysis

(b) Transient Analysis

(c) AC Analysis

(d) DC Sweep **Theory :**

LTSPICE is a general-purpose circuit-simulation program for nonlinear DC, nonlinear transient and linear AC analysis. As outlined above, it solves the network equations for the node voltages. The program is equally suited to solves linear as well as nonlinear electrical circuits. Circuits can contain:

- resistors, capacitors, inductors, mutual inductors,
- independent voltage and current sources,
- dependent voltage and current sources,
- transmission lines,
- the most common semiconductor devices:
  - diodes,
  - bipolar junction transistors (BJTs),
  - junction-field effect transistors (JETs),
  - metal-oxide-semiconductor field effect transistors (MOSFETs),
  - metal-semiconductor FETs GaAs (MESFETs); –special devices and integrated circuits.

Any general-purpose circuit simulation program must to give the following three basic solutions: bias point (OP), frequency response (AC) and transient response.

The DC analysis part of the program computes the bias point of the circuit with capacitors disconnected and inductors short-circuited. SPICE uses iterations to solve the

nonlinear network equations; nonlinearities are due mainly to the nonlinear currentvoltage (I-V) characteristics of semiconductor devices.

The AC analysis mode computes the complex values of the node voltages of a linear circuit as a function of the frequency of a sinusoidal signal applied at the input.

For nonlinear circuits, such as transistor circuits, this type of analysis requires the smallsignal assumption; that is, the amplitude of the excitation sources are assumed to be small compared to the thermal voltage for BJTs ($V_{in} << V_{th}$= 25mV, for small distortions). Only under this assumption can the nonlinear circuit be replaced by its linearized equivalent around the DC bias point.

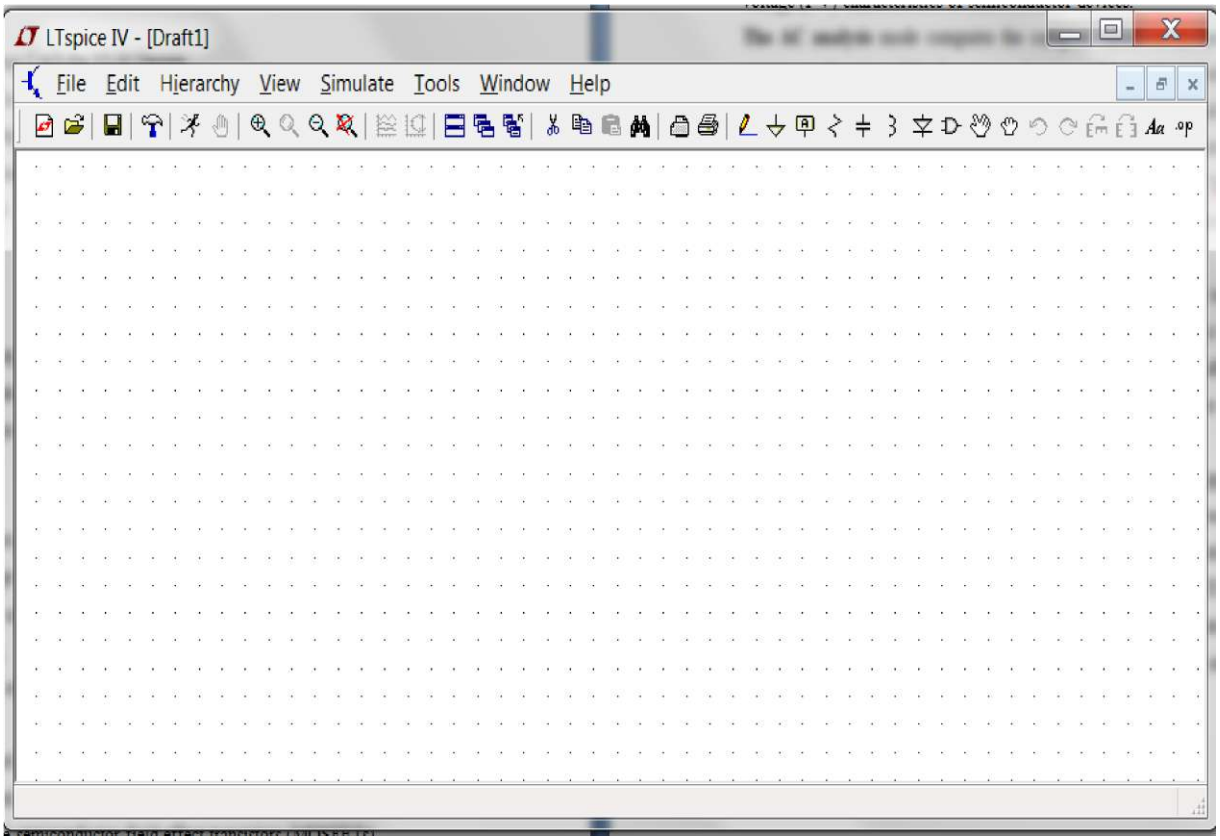


Fig 1: LT Spice Schematic Capture Window

The transient analysis mode computes the voltage waveforms at each node of the circuit as a function of time. This is a large-signal analysis: no restriction is put on the amplitude of the input signal. Thus the nonlinear characteristics of semiconductor devices are taken

into account. More types of analysis, associated with the above three basic simulation modes, are available in SPICE.

Actual circuits also require expensive equipment like power supplies, signal generators and oscilloscopes. It may be difficult to physically breadboard every circuit you encounter. You can spend hours building an actual circuit and only get a simple concept from it, whereas, SPICE provides the insight in minutes. SPICE can be your "virtual" breadboard. Even if you have a short time to spare, you can cover several circuit principles and applications. Here LTSpice is used for design and simulation.

Electric CAD :-

A state−of−the−art computer−aided design system for VLSI circuit design. Electric designs MOS and bipolar integrated circuits, printed−circuit−boards, or any type of circuit you choose. It has many editing styles including layout, schematics, artwork, and architectural specifications. A large set of tools is available including design−rule checkers, simulators, routers, layout generators, and more.

Electric interfaces to most popular CAD specifications including EDIF, LEF/DEF,

VHDL, CIF and GDS. The most valuable aspect of Electric is its layout−constraint system, which enables top−down design byenforcing consistency of connections.

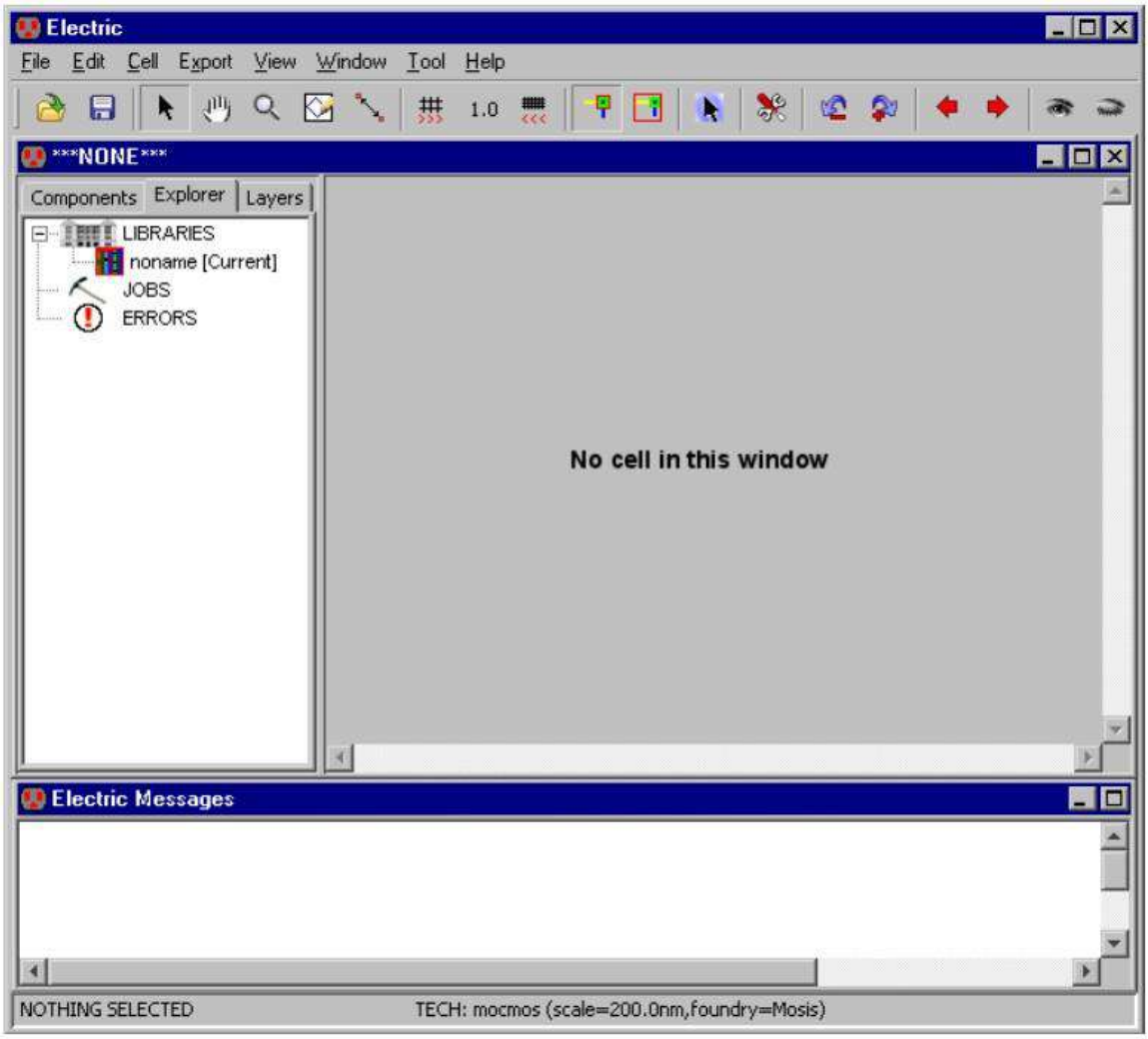
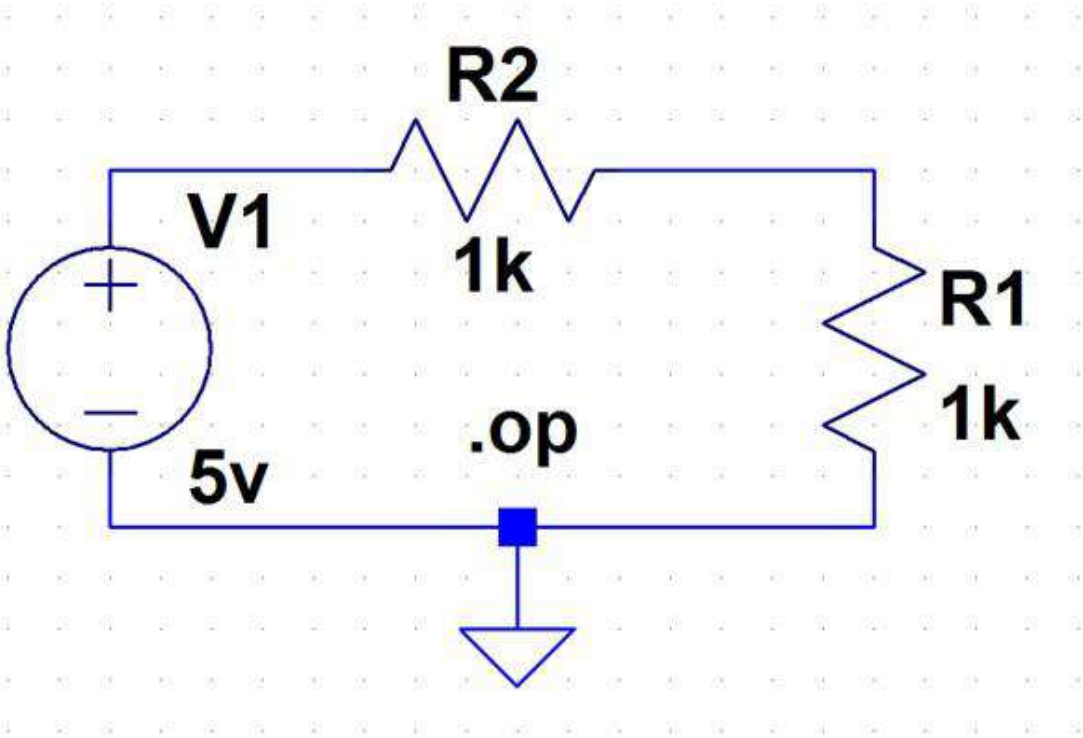


Fig 2: Electric CAD schematic and Layout capture window

Design and Simulation Results :



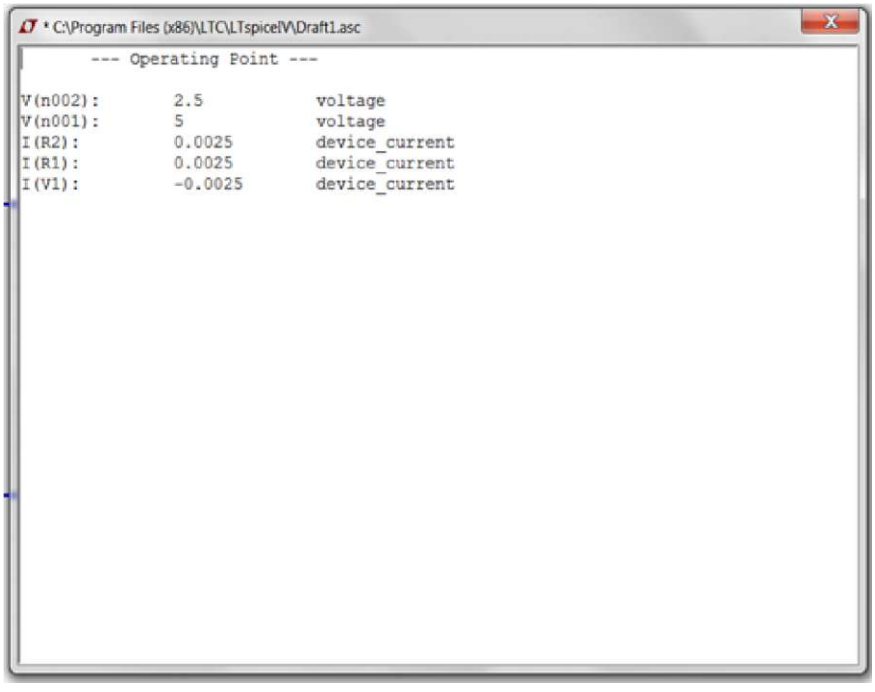
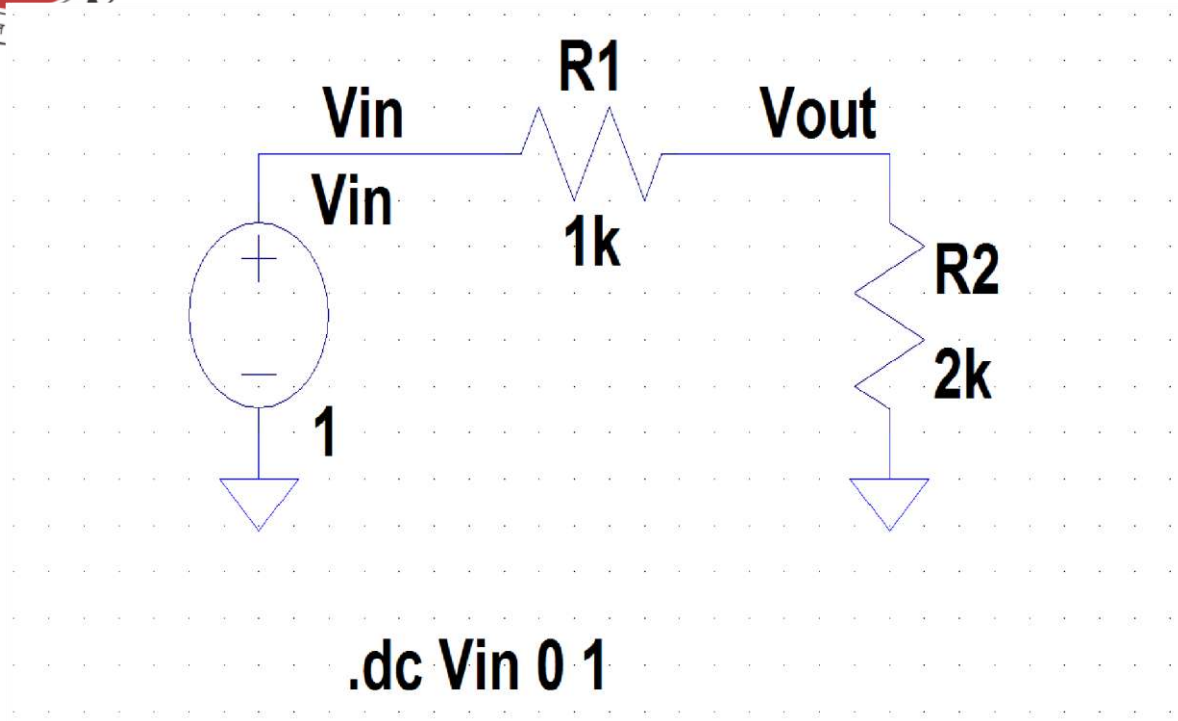


Fig 3: Resistance divider schematic and operating point analysis results



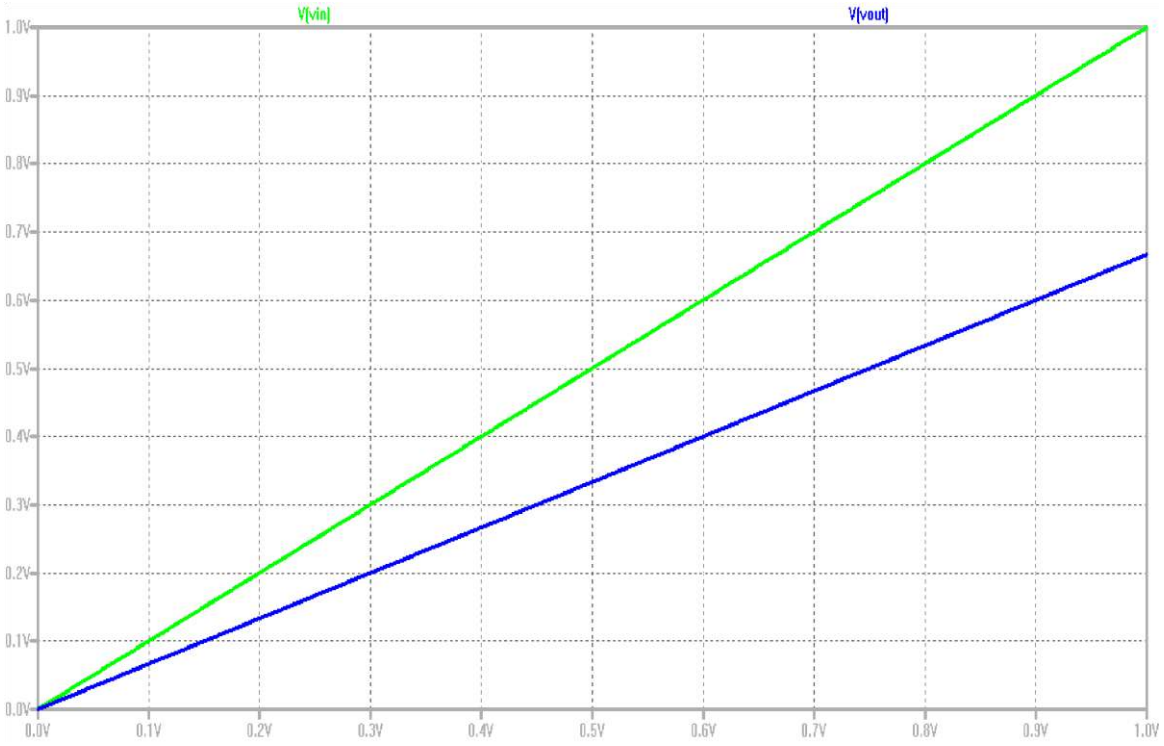
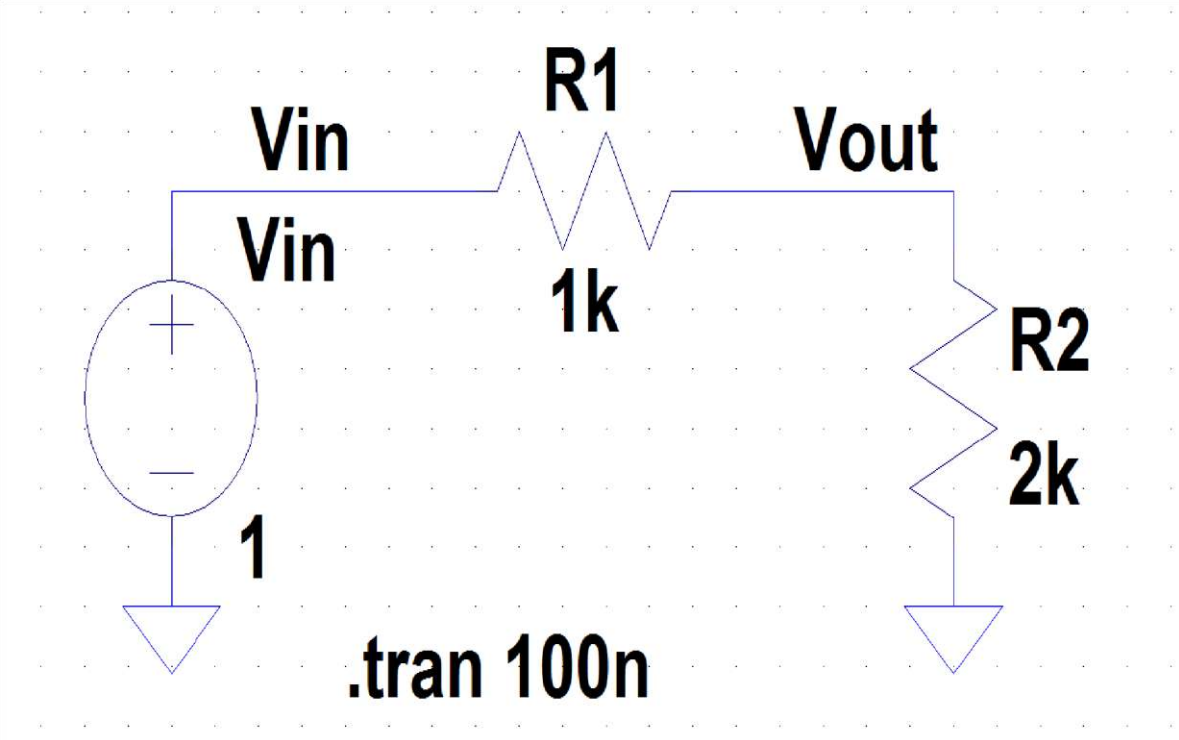


Fig 4: Resistance divider schematic and dc sweep analysis plot


R1
Vin
Vout
Vin
1k
R2
2k
1
.tran 100n


V(vin)
V(vout)
1.02V
0.99V
0.96V
0.93V
0.90V
0.87V
0.84V
0.81V
0.78V
0.75V
0.72V
0.69V
0.66V
0ns
10ns
20ns
30ns
40ns
50ns
60ns
70ns
80ns
90ns
100ns

Fig 5 : Resistance divider schematic and transient analysis plot

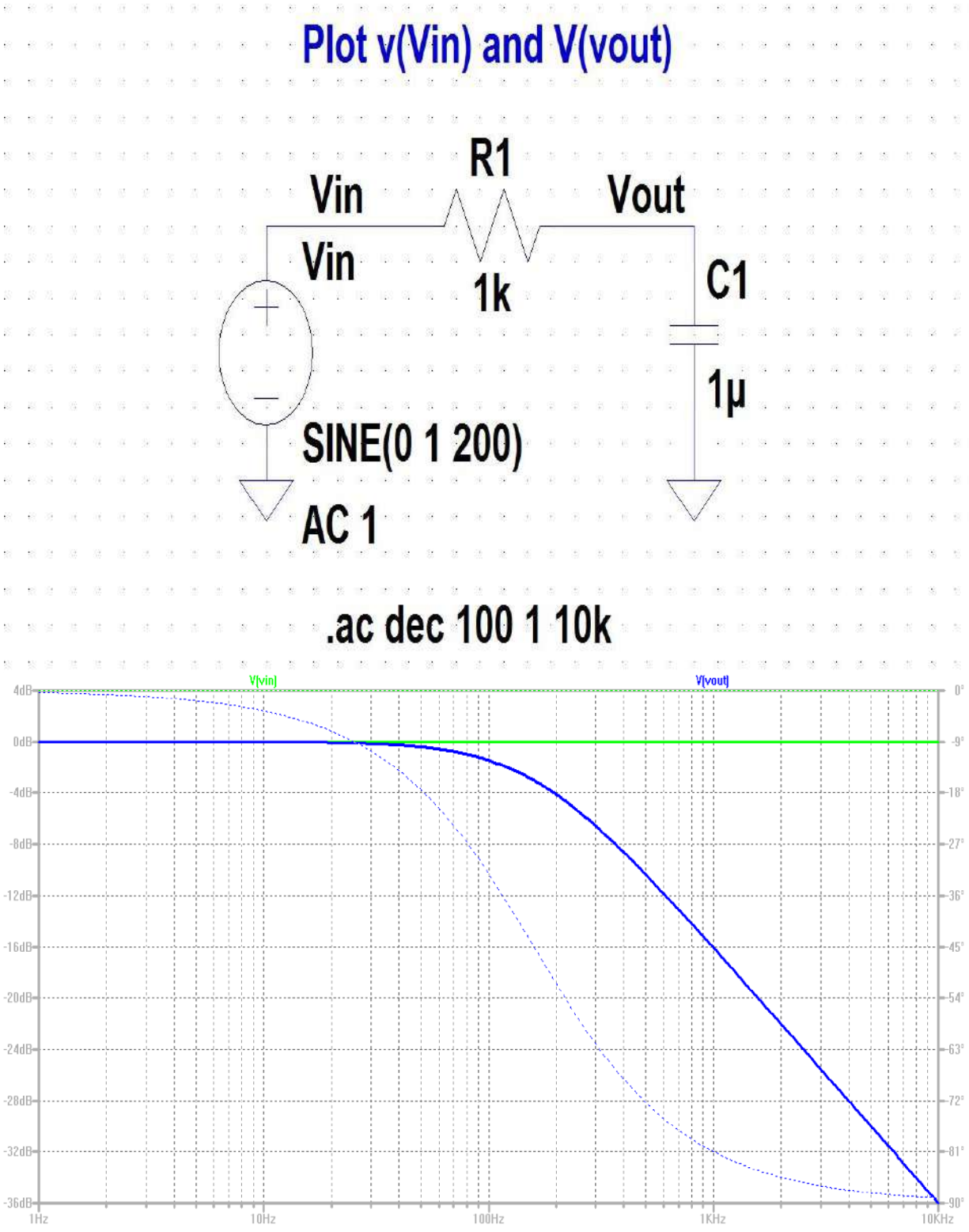
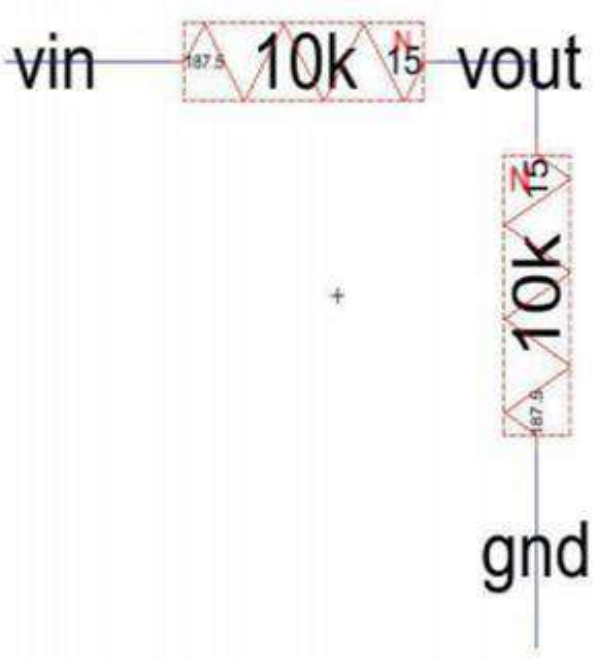


Fig 6 : Resistance divider schematic and transient analysis plot

Design and Simulation Results :



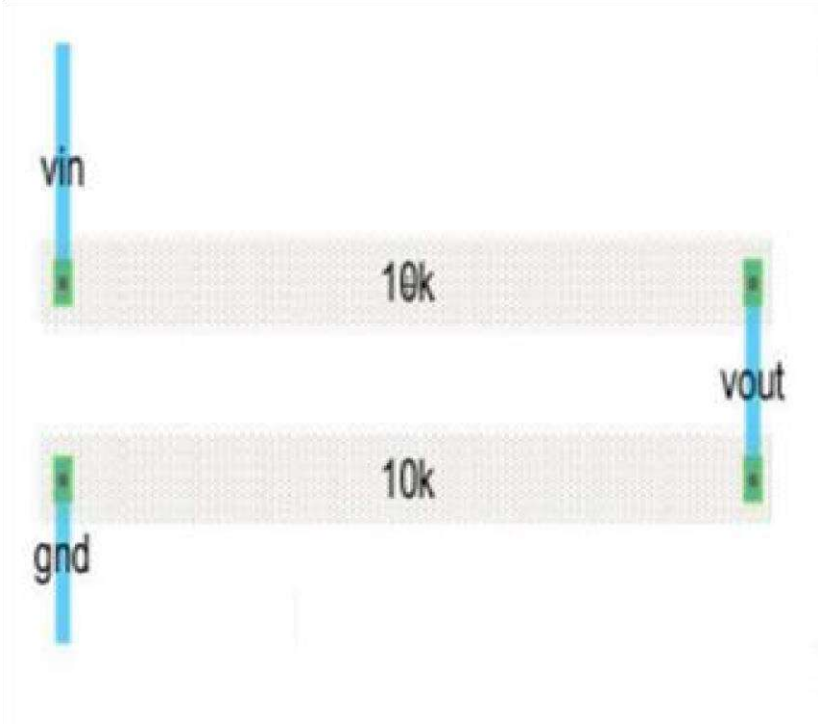


Fig 7 : Resistance divider schematic and Layout capture

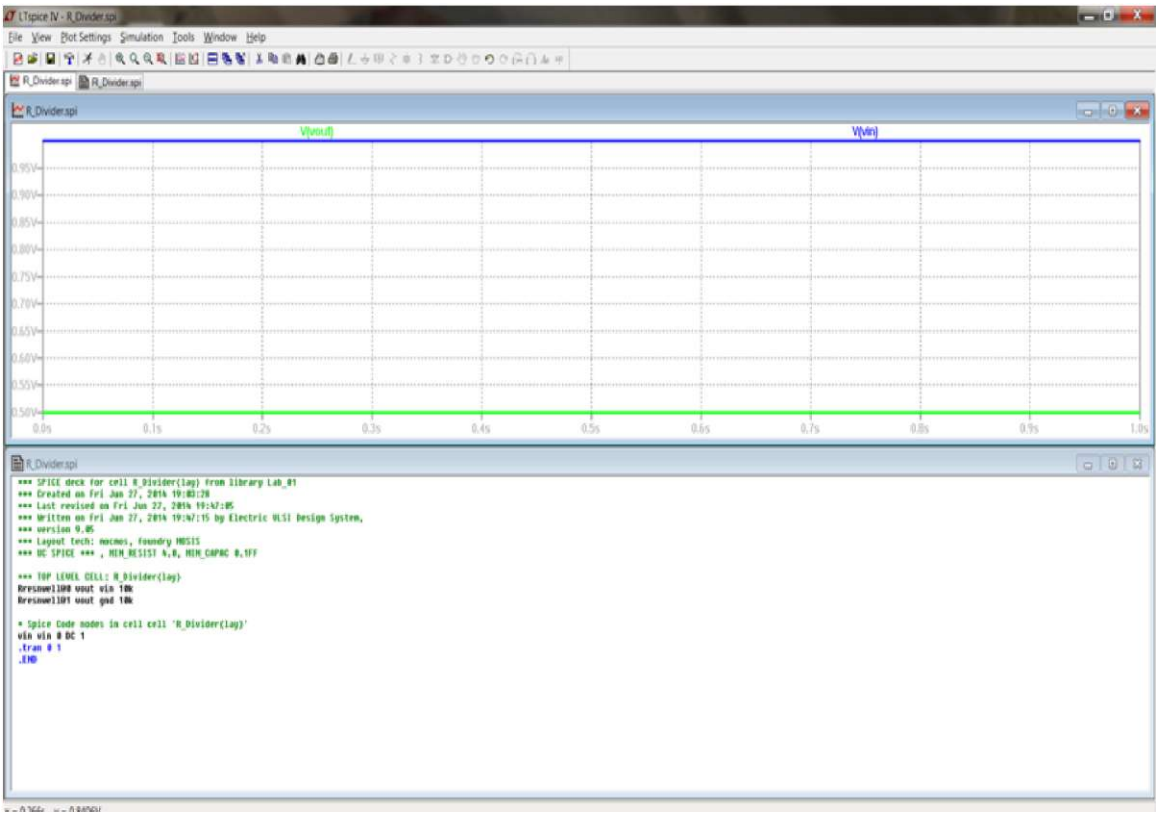


Fig 8 : Transient Analysis plot for n-well resistance divider **Conclusion / Summary :**

Simulation softwares for VLSI flow have been studied and examples have been implemented.

(Both Backend and Frontend)

Softwares flow has been studied are as under-

1. LTSpice

2. Electric CAD

Example Implemented

Voltage Divider

Viva Questions

1. What is simulation ? why it is important ?
2. What is circuit simulation ?
3. What is SPICE ?
4. What are the various type of design entries in VLSI design ?
5. Write the syntax for
   - 5.1 Operating point analysis
   - 5.2 AC Analysis
   - 5.3 DC Analysis
   - 5.4 Noise Modelling
   - 5.5 Transient Analysis
   - 5.6 Sinusoidal input
   - 5.7 Pulse Input
6. What is Layout ?
7. What is Process Technology ?
8. What are various Design rule check ?
9. Explain LTSpice Design flow ?
10. Explain Electric CAD Design Flow ?

Experiment -3

Make an ideal Op-Amp sub circuit and symbols and use it as the following and perform necessary analysisand MOS circuit analysis

Aim/Objective :

3.1 Make an ideal Op-Amp sub circuit and symbols and use it as the following and perform necessary analysis

a. Inverting Amplifier
b. Non Inverting Amplifier
c. Adder
d. Substractor
e. Integrator
f. Differentiator

3.2 Simulate the following MOS circuits using LTSpice

a. Inverter
b. Ring Oscillator
c. Gates

Theory :

To simulate an op amp in LTSpice, begin by opening the component library, searching for "UniversalOpamp2" and clicking ok

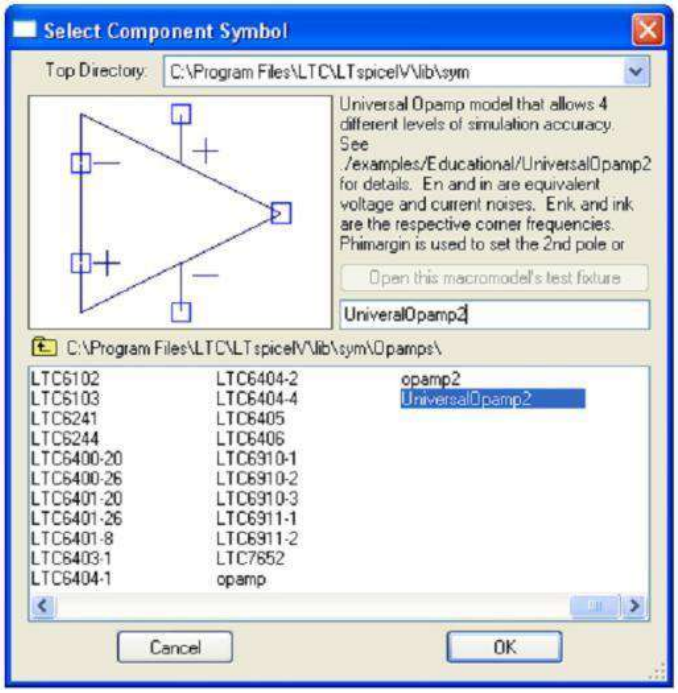


Fig 1: LT Spice Symbol Universal OpAmp

Connect the positive, negative, and output terminals of the op amp to the rest of the circuit. An additional step before simulating most integrated circuits (ICs) such as an op amp is to power the device. This is an important step because an op amp is only able to output a value between the ranges of voltages it is powered with. In this example the output signal should be an inverted and amplified signal to five times the size of the input waveform.

Power the positive rail of the op amp with a 100V DC source. This value can change depending on the experiment, but for this example it is assumed infinite. Connect the negative rail of the op amp to ground. In this simulation it is clear to see that the input voltage varies between -5V and 5V as expected. The output voltage is inverted and amplified to five times the size of the input waveform, but only for half of the time. This is not the desired output waveform. What happened was that although the op amp was able to supply +25V with an input voltage of -5V (because the positive rail of the op amp was powered with +100V) it was unable to supply -25V with an input voltage of +5V. This is because the negative rail of the op amp was connected to ground, which means that the lowest voltage this op amp can supply is 0V.
The behavior of the output waveform, which suddenly maintains a constant voltage as the result of undesired limitations is known as “clipping.” This is a common problem when dealing with op amps and can either be solved by introducing a DC offset to shift the signal up (in this case an output DC offset of +25V would be required to avoid clipping) or to change the device limitations.

In this simulation we will change the device limitations by powering the negative rail of the op amp with a -100V source. This will allow the output signal to vary between +100V and -100V. Place another voltage source with the positive terminal connected to the negative rail of the op amp, the negative terminal to ground, and a value of -100V as shown below: Re-simulate the circuit. As before measure the input voltage at “Vin” and t

ion

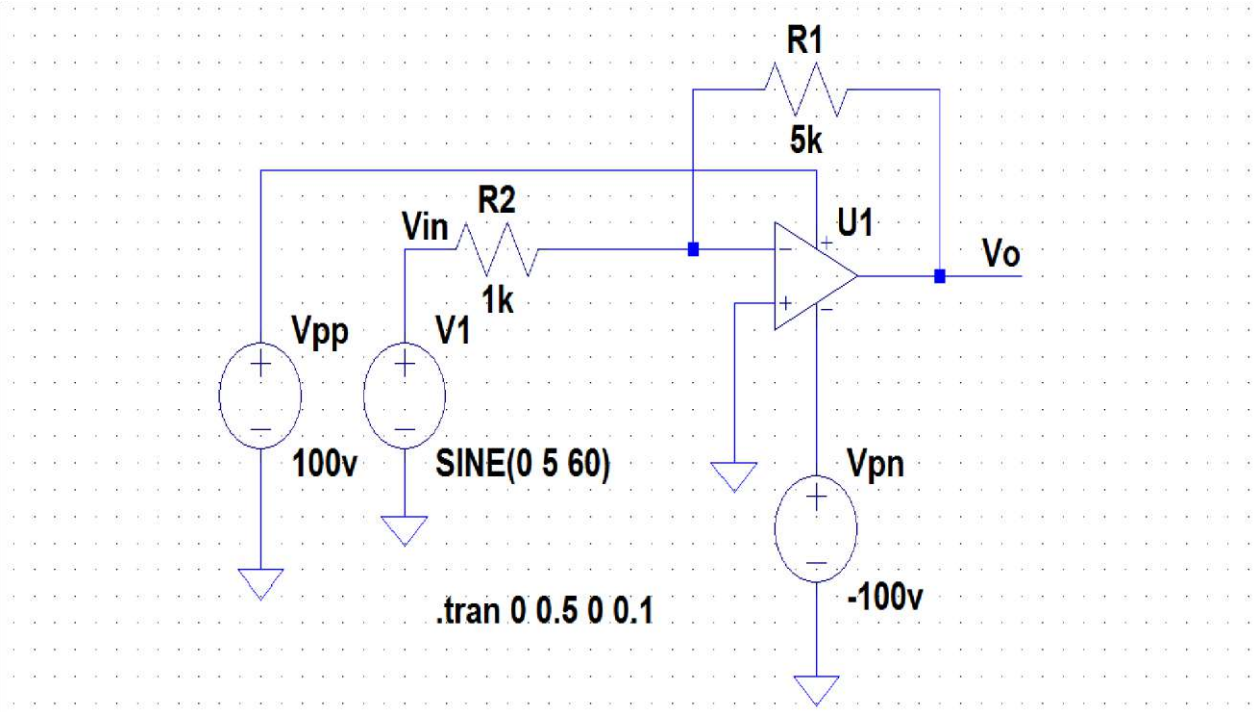


Figure 1: Schematic of Ideal Opamp simulation

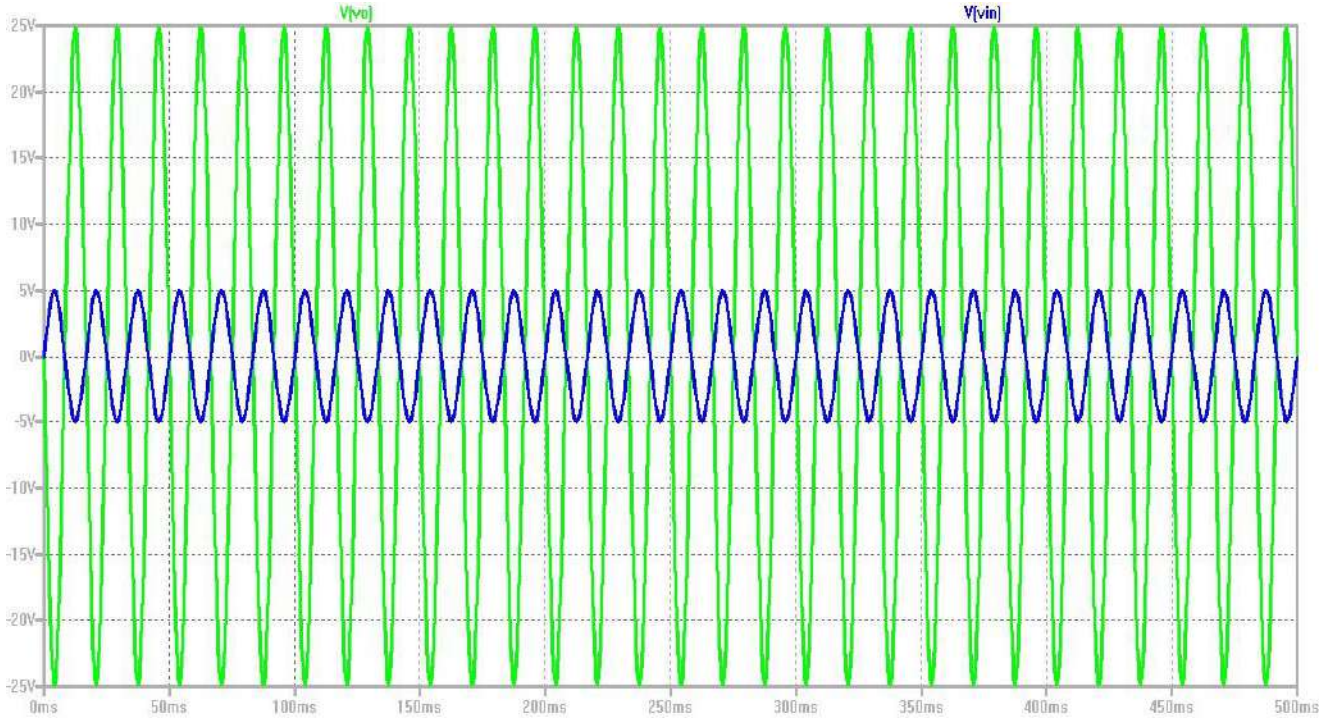


Figure 2: Plot for Vout vs Vin for Ideal Opamp Schematic in figure 1

Design and Simulation Results :

We are basically using a simple approach here, what we will be using a voltage controlled current source with a parallel resistance to implement input voltage and output voltage scenario.

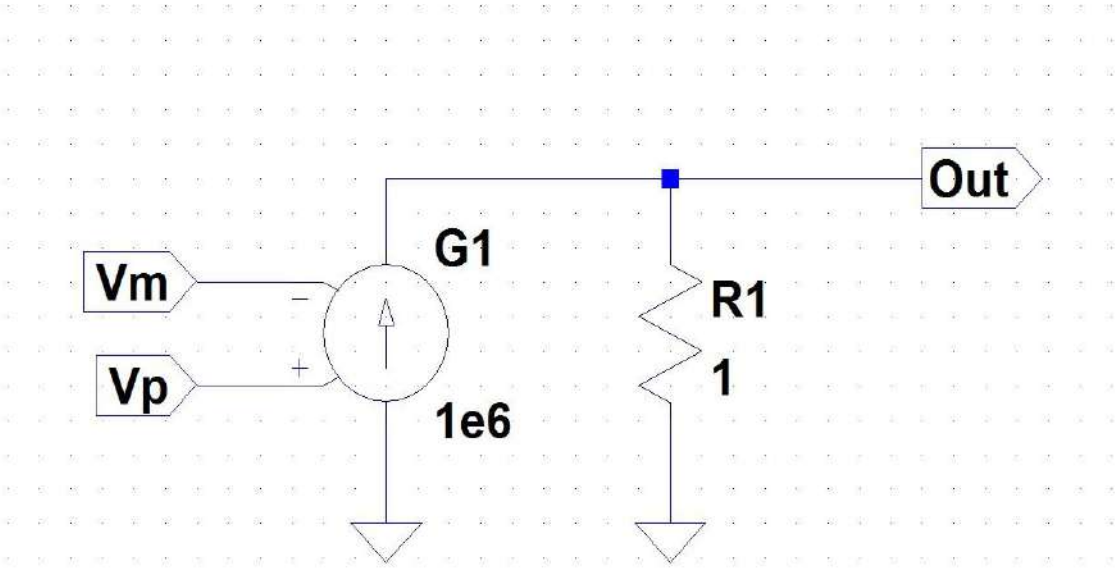


Figure 3: Ideal Operational Amplifier using VCCS

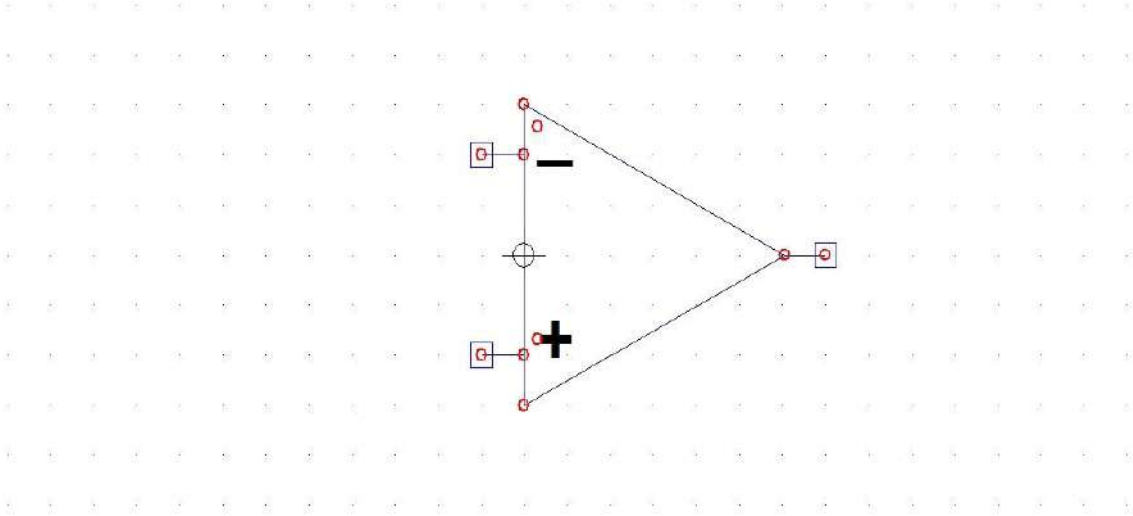


Figure 4: Symbol for Ideal Operational Amplifier

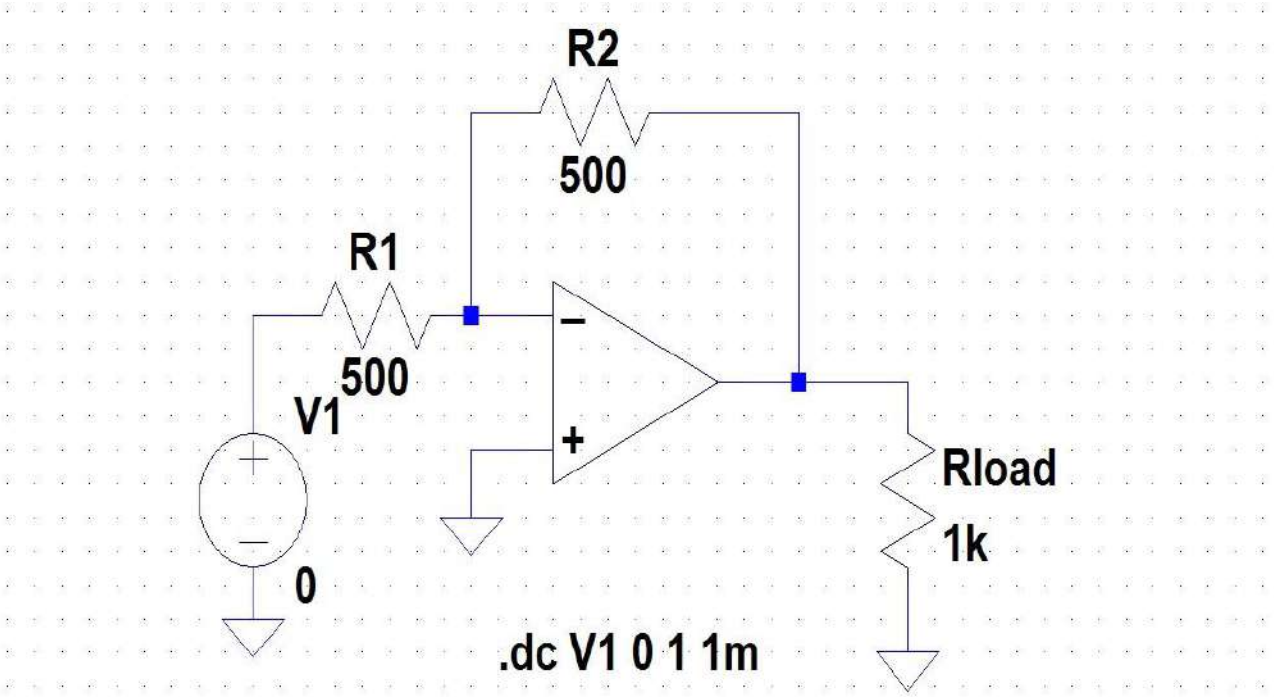


Figure 5: Ideal Opamp in inverting configuration

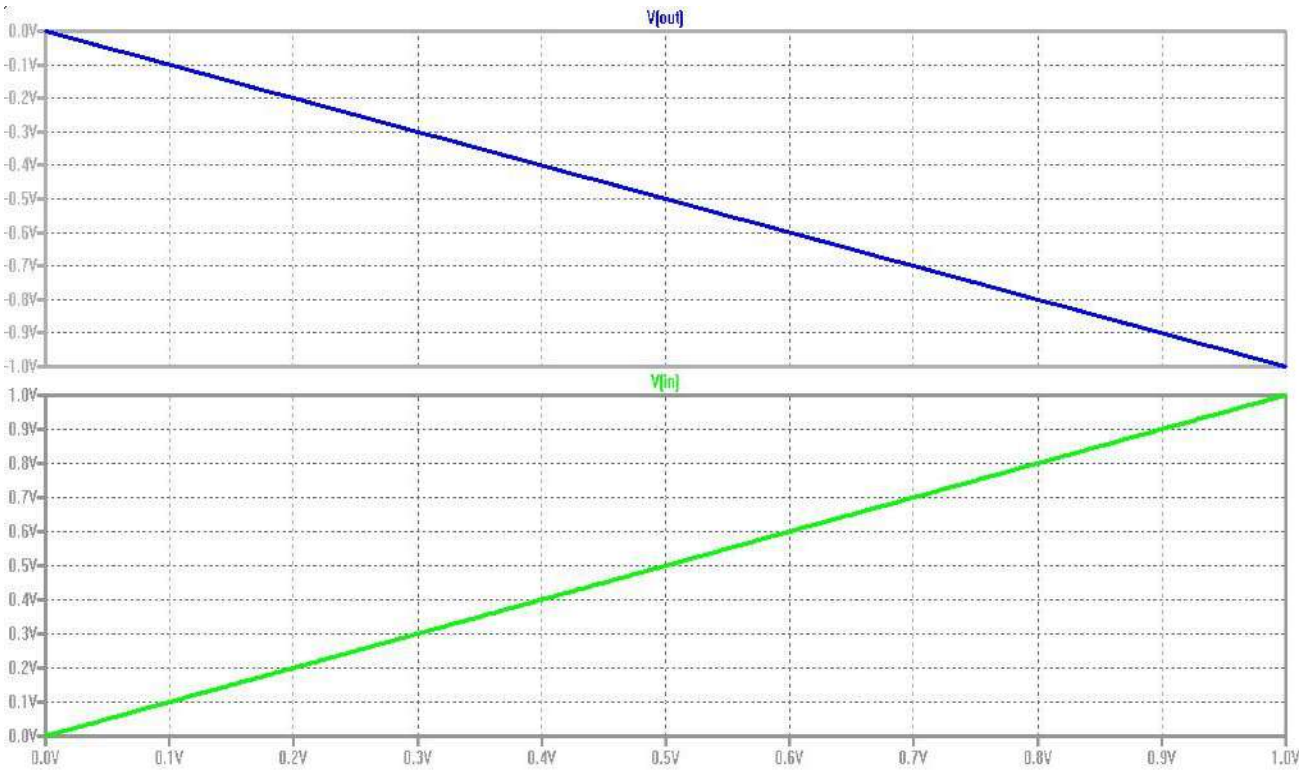


Figure 6: Plot for Ideal Opamp in inverting configuration

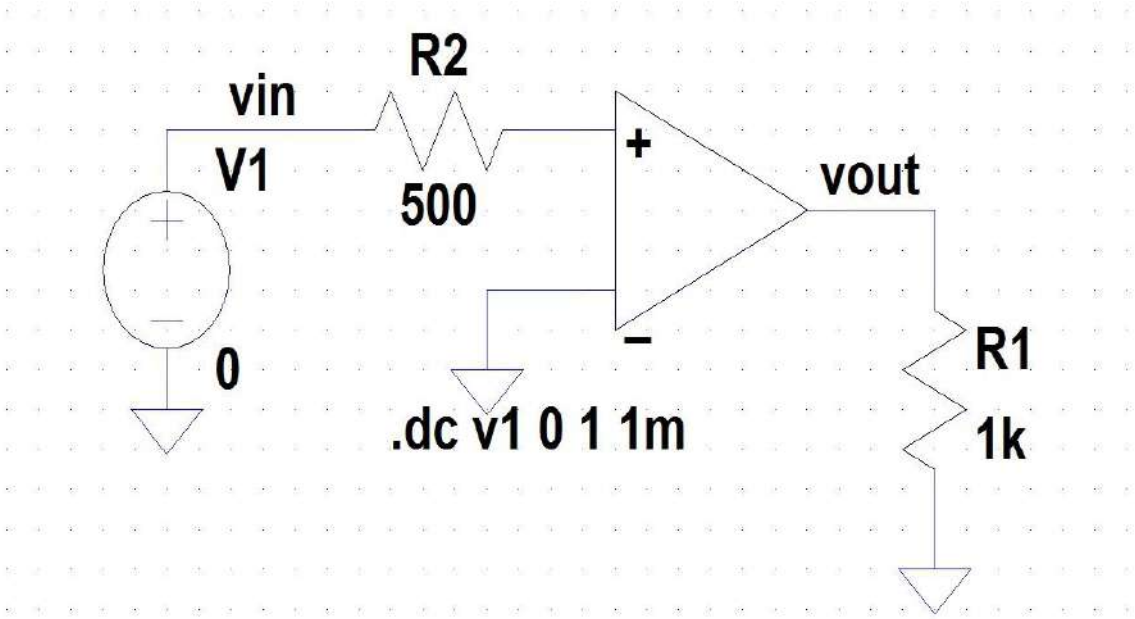


Figure 7: Ideal Opamp in non-inverting configuration

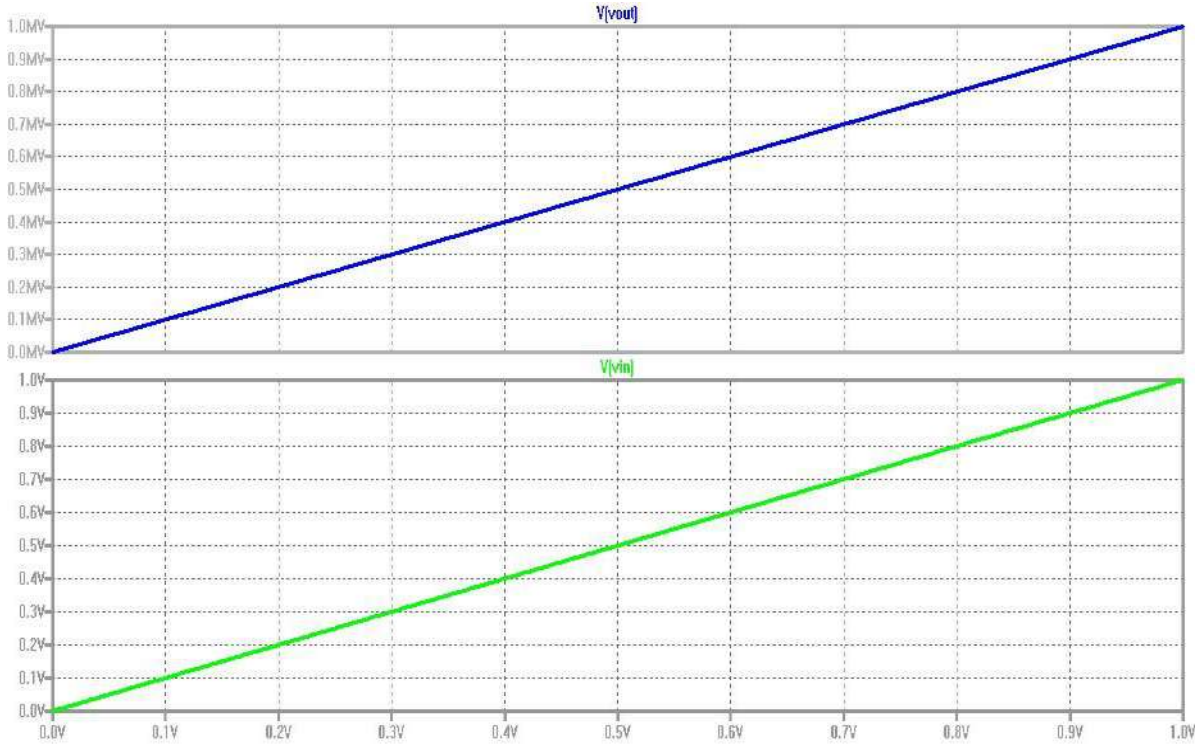


Figure 8: Plot for Ideal Opamp in non-inverting configuration

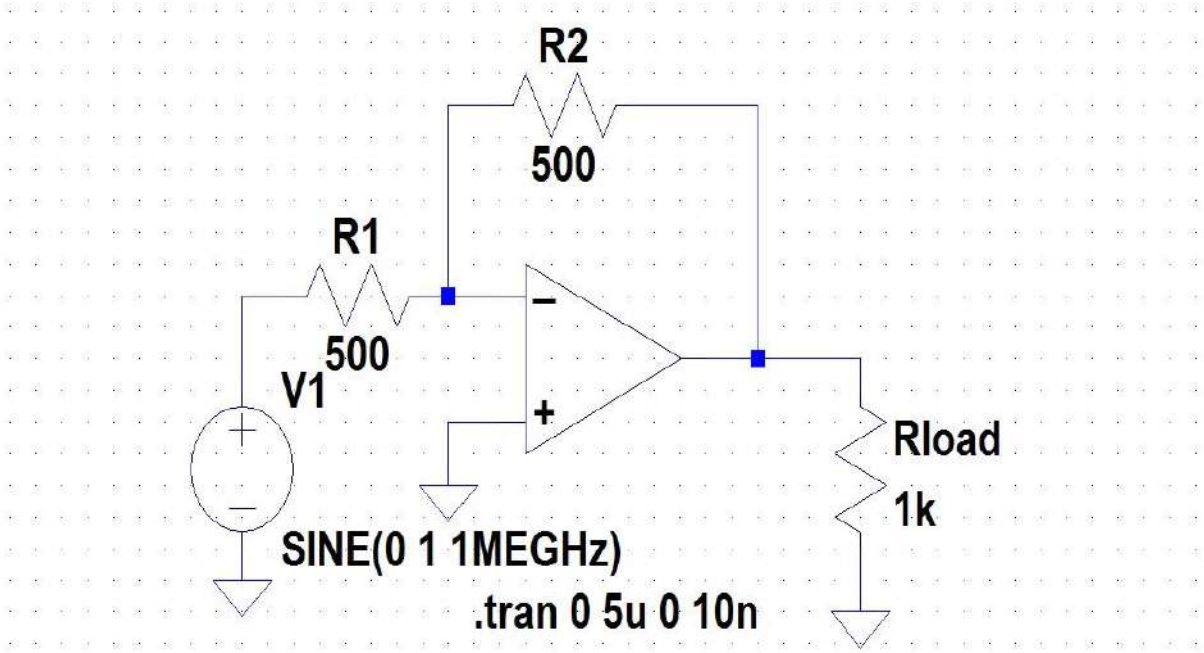


Figure 9: Schematic for Ideal Opamp in inverting configuration

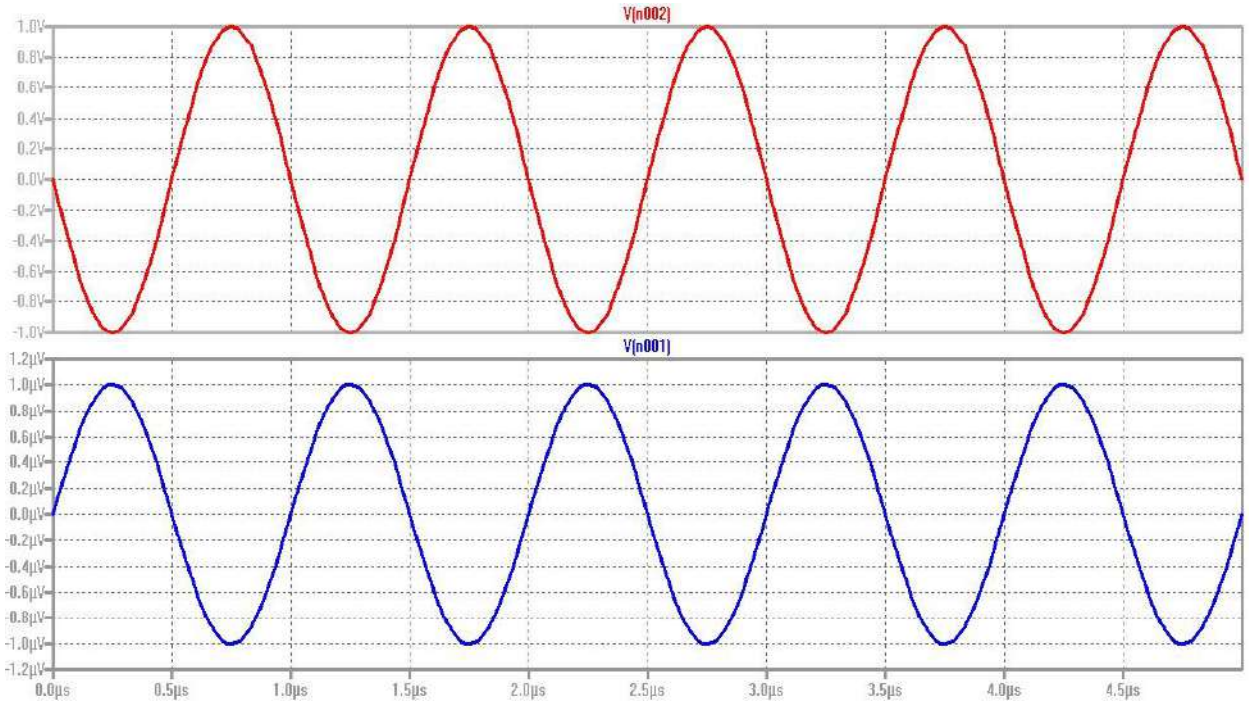


Figure 10: Plot for Ideal Opamp in inverting configuration

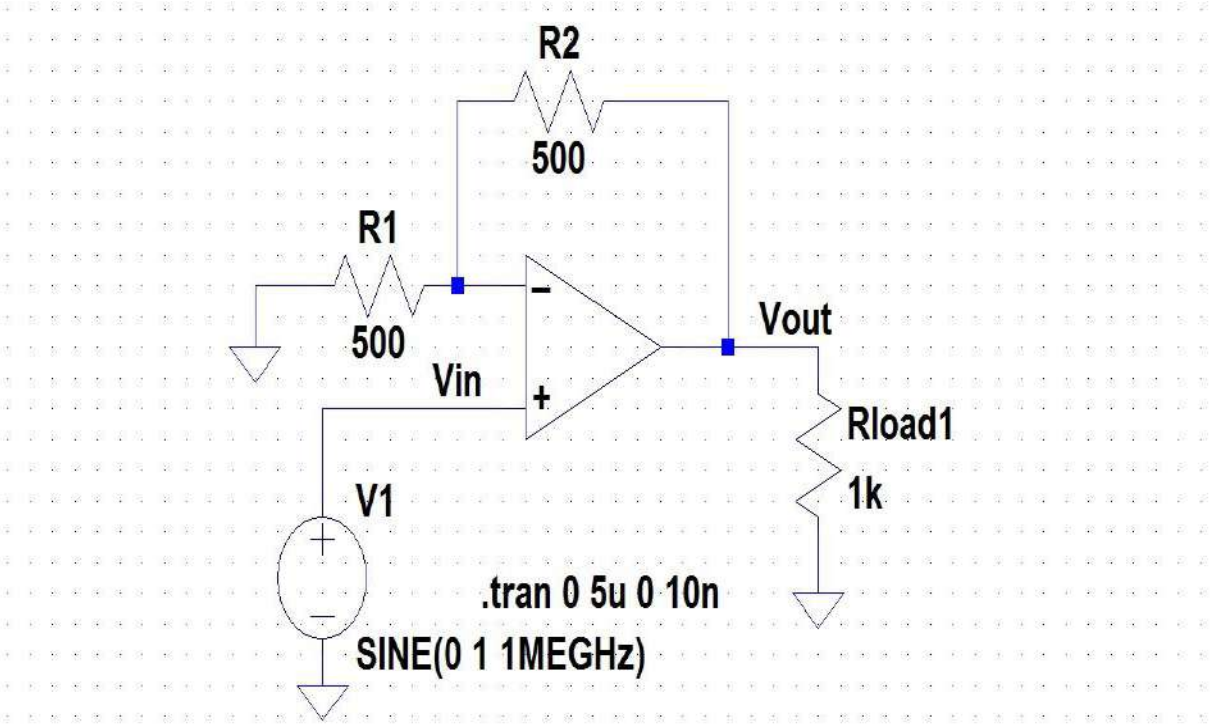


Figure 11:Schematic for Ideal Opamp in non-inverting configuration

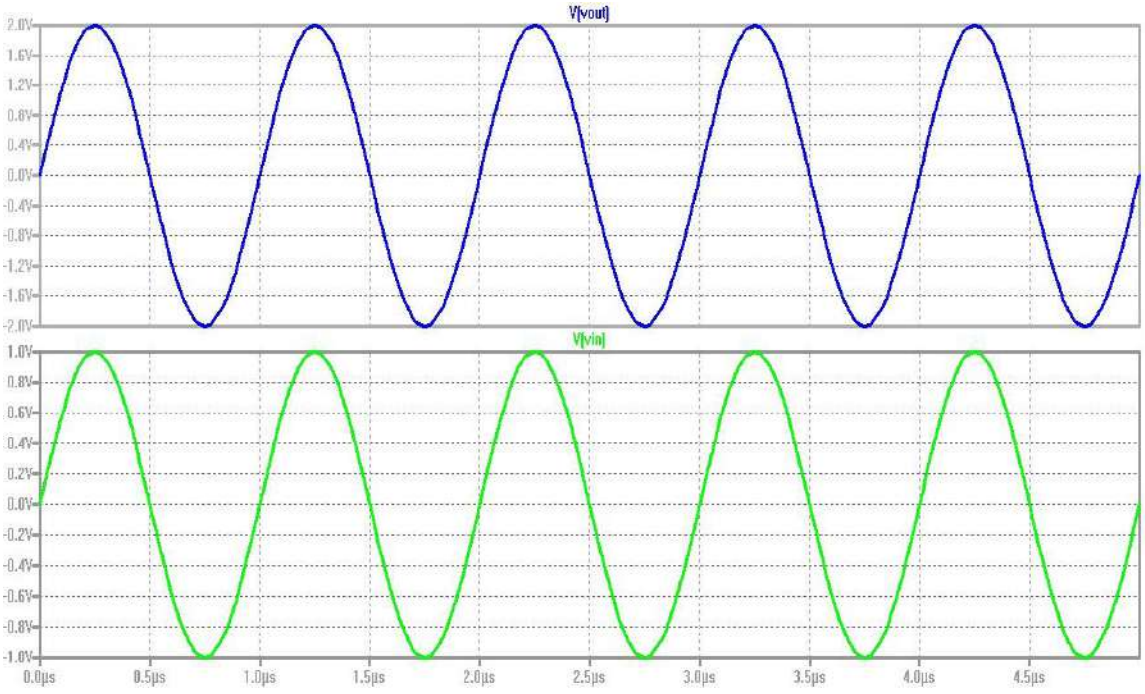


Figure 12: Plot for Ideal Opamp in non-inverting configuration

Design and Simulation Results :

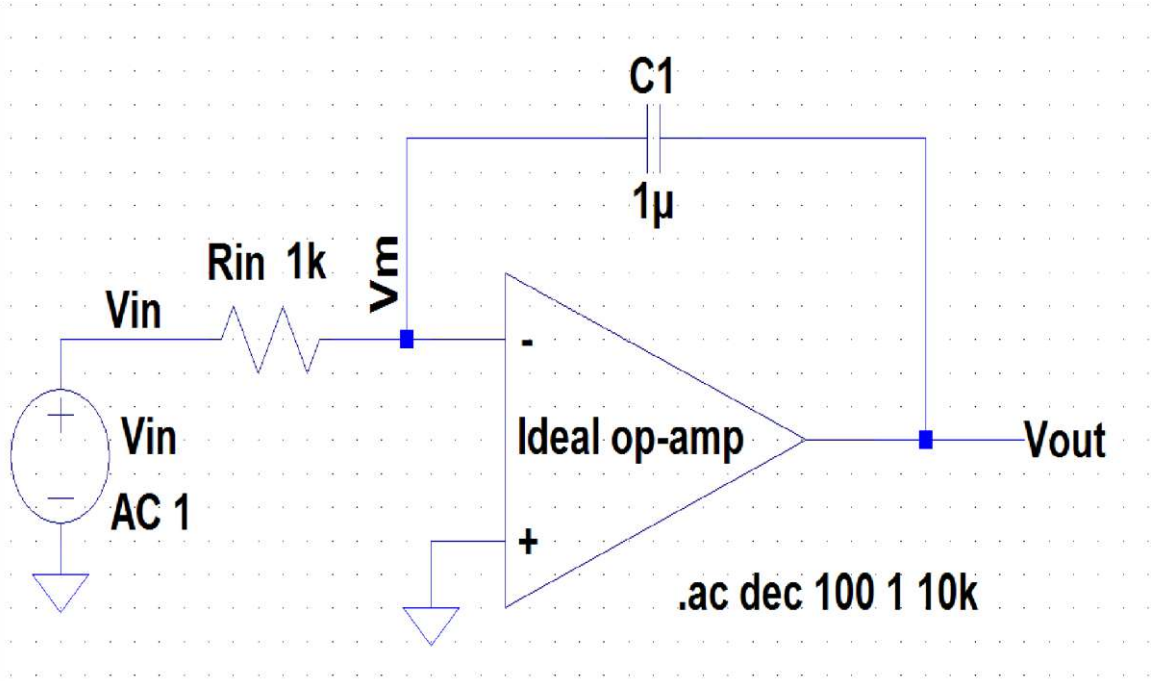


Figure 13: Schematic for Ideal Opamp used as a Integrator

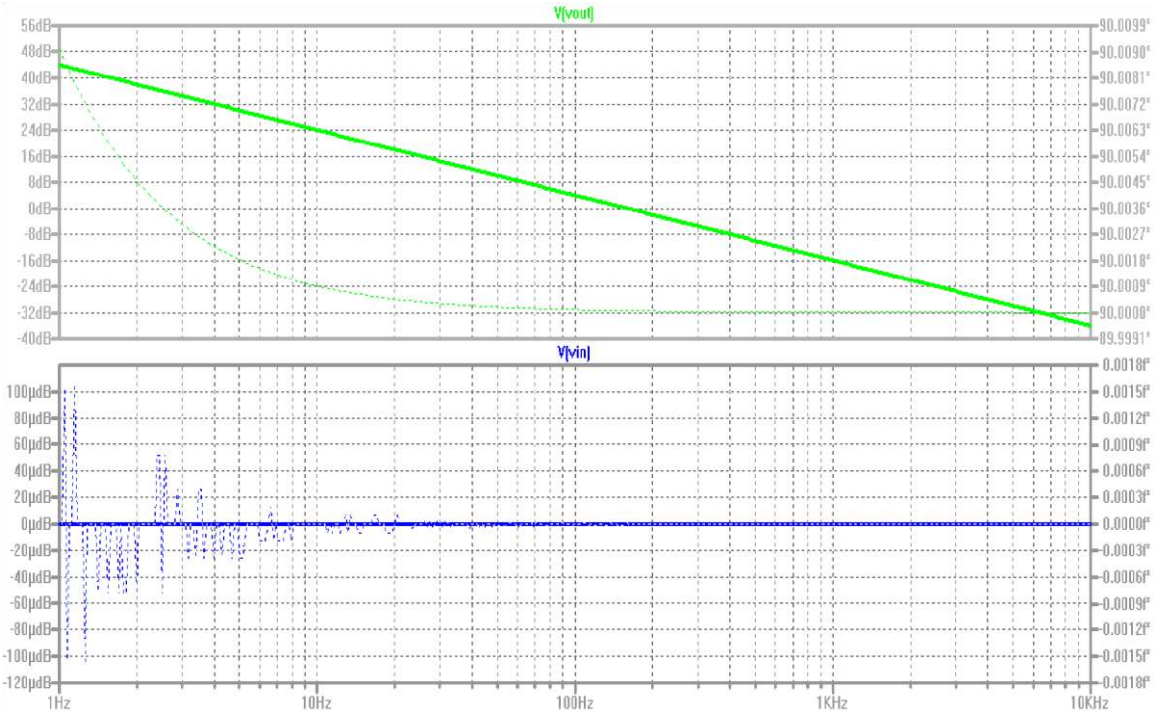


Figure 14: Plot for Ideal Opamp used as a Integrator

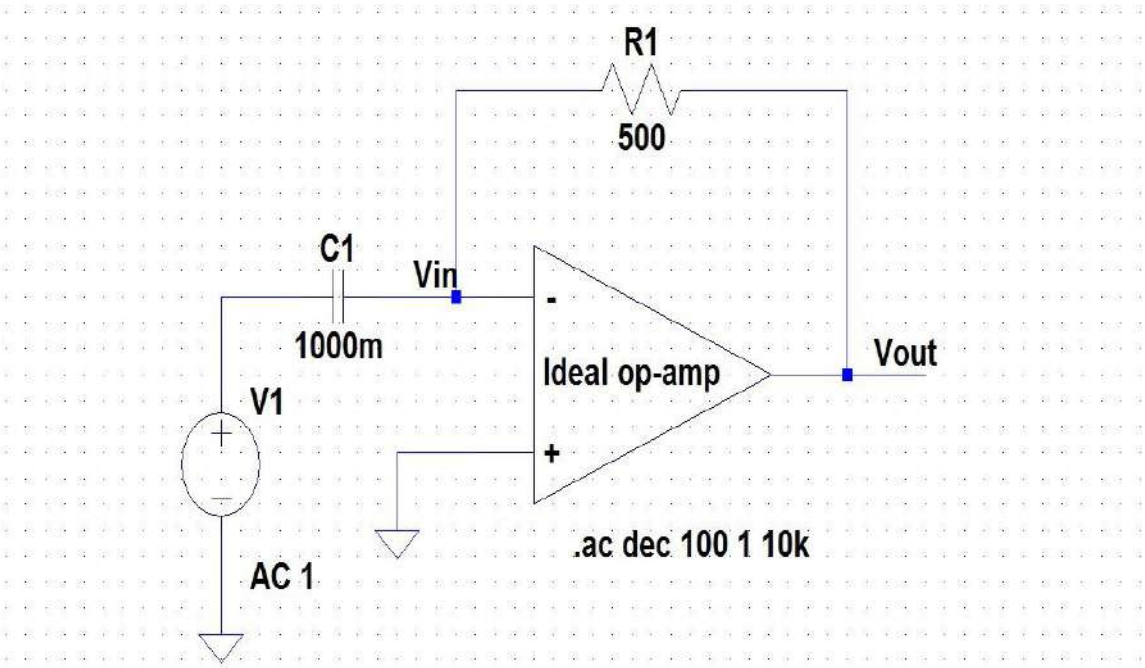


Figure 15: Schematic for Ideal Opamp used as a Differentiator

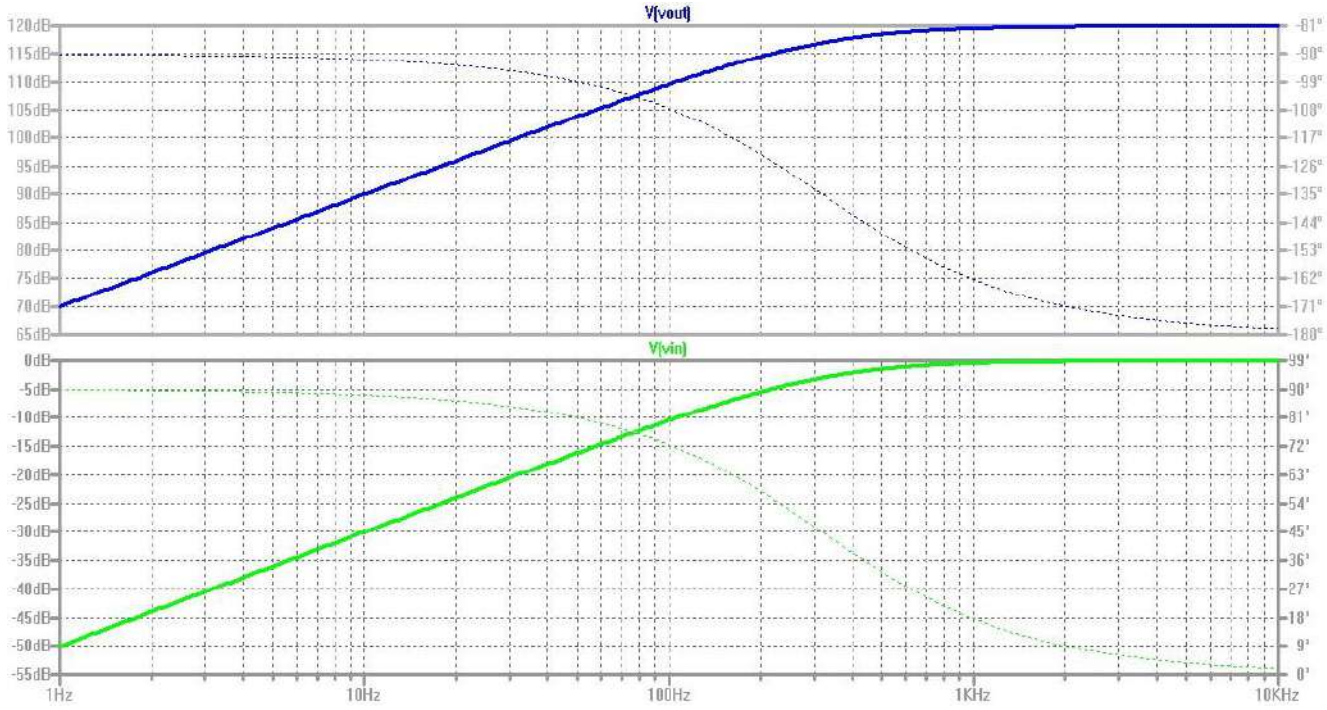


Figure 16: Schematic for Ideal Opamp used as a Integrator

MOS Circuits simulation using LTSpice

LT Spice software allows users to define their own devices and use their own models for simulations. Spice is the most commonly used circuit simulations. To run simulations of MOSFETs we need to at least set the values of parameters L (channel length), W (channel width), VT0 (zero -bias threshold voltage), KP (transconductance, μn/p , Cox,), and LAMBDA (channel -length modulation coefficient.

When SPICE (not LTspice) was first created, the programmers gave the user a specific number of characteristics to define certain components. In the case of the MOSFET, this included the gate source turn on voltage, the transconductance, the resistance of the gate, source and drain connections etc. These are known as Level 1 parameters and define the most important parameters of the MOSFET. In later years, the MOSFET manufacturers wanted to further characterise their MOSFETs and not be restricted by the fixed list of parameters given to them by the writers of SPICE. They therefore turned to the .SUBCKT definition to allow them to expand the list of parameters. These are known as Level 2 and Level 3 parameters and describe characteristics of the MOSFET not defined

in the original SPICE definition of a MOSFET. However in making the model more complicated, they slowed down the simulation time of the MOSFET.

LTspice therefore uses the simpler .MODEL statement to define the characteristics of a MOSFET. If using a 3rd party MOSFET model results in very slow simulation performance, it is probably because the model is defined using the .SUBCKT model and includes many parameters that are not necessary in getting an idea of the circuit performance.

Design and Simulation Results :

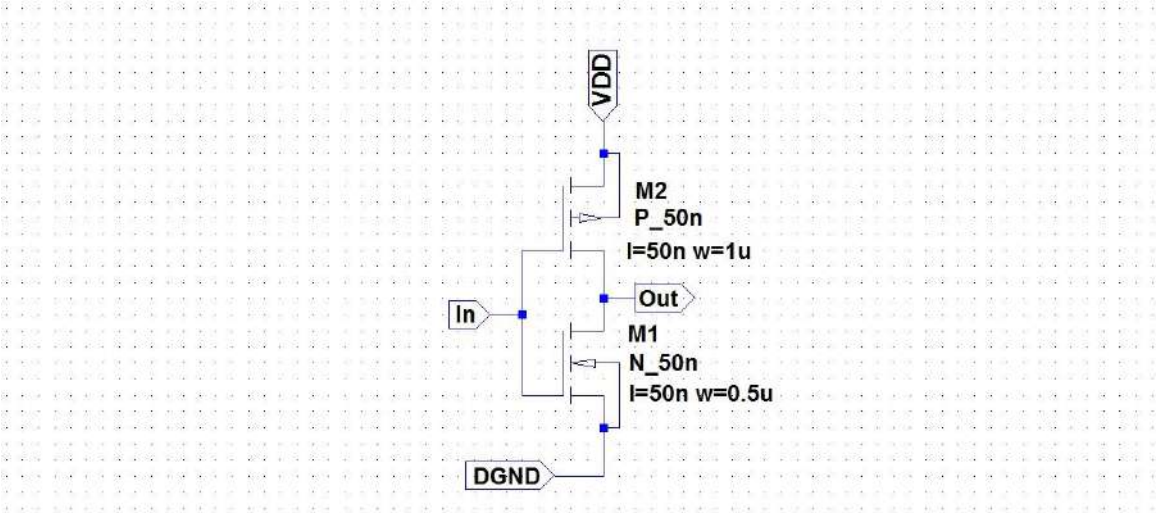


Figure 17: Schematic for Digital Inverter

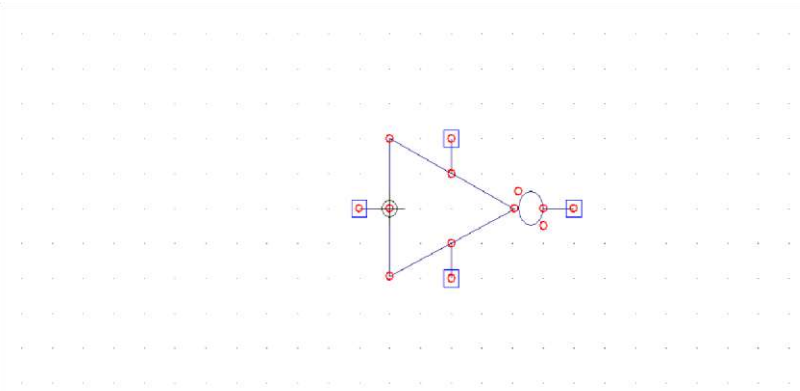


Figure 18: Schematic for Digital Inverter

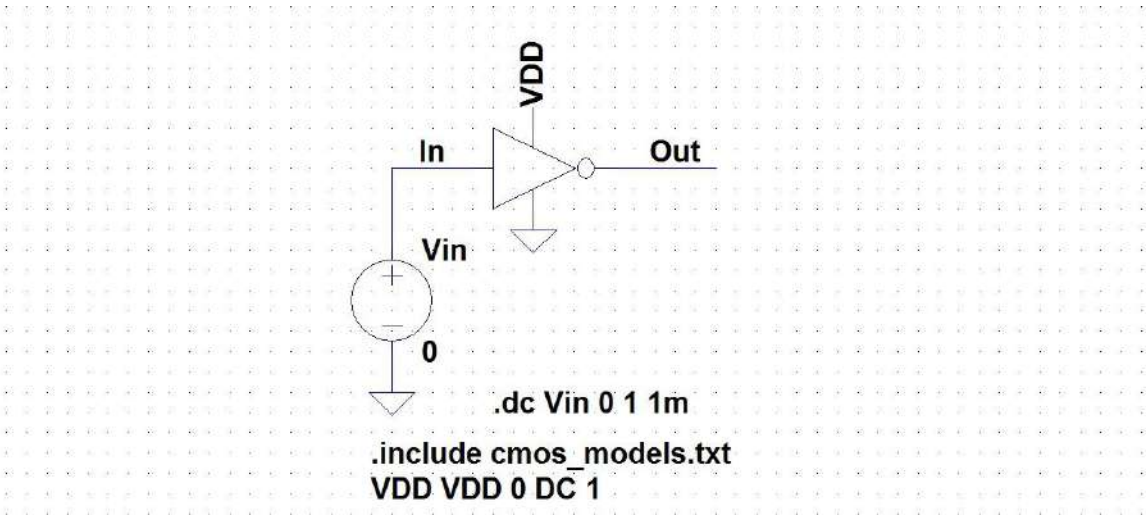


Figure 19: DC Simulation for Digital Inverter

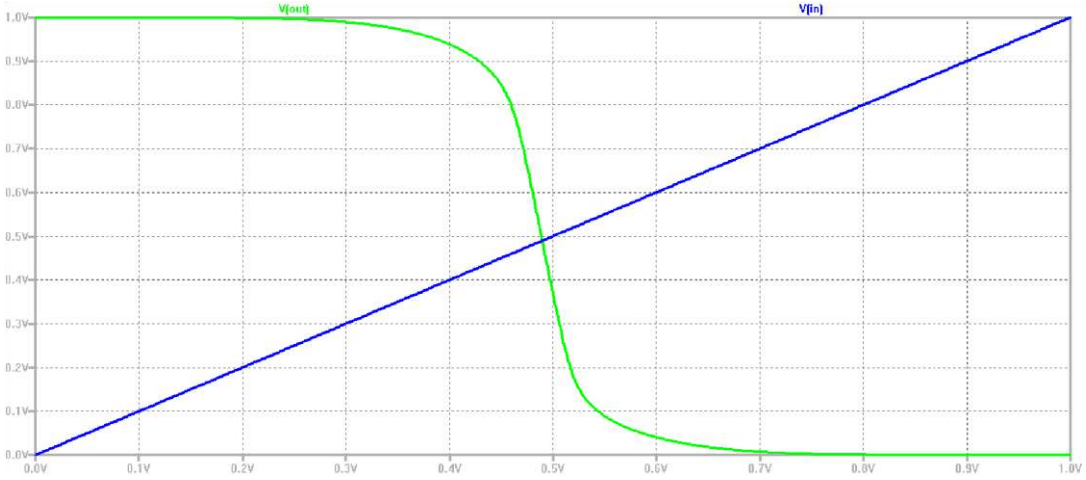


Figure 20: DC Simulation plot for CMOS Inverter

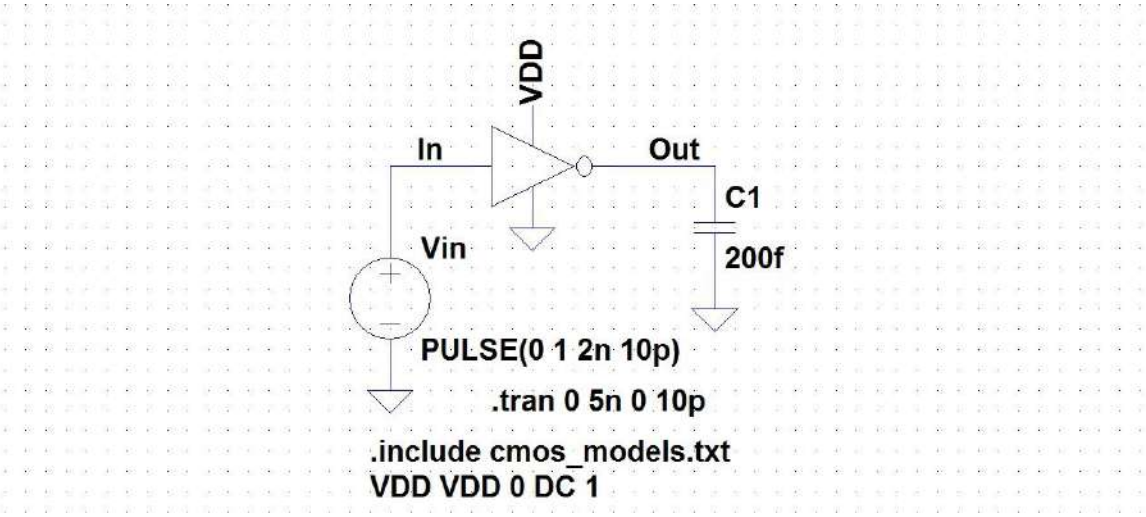


Figure 21: Schematic for Digital Inverter using variable load

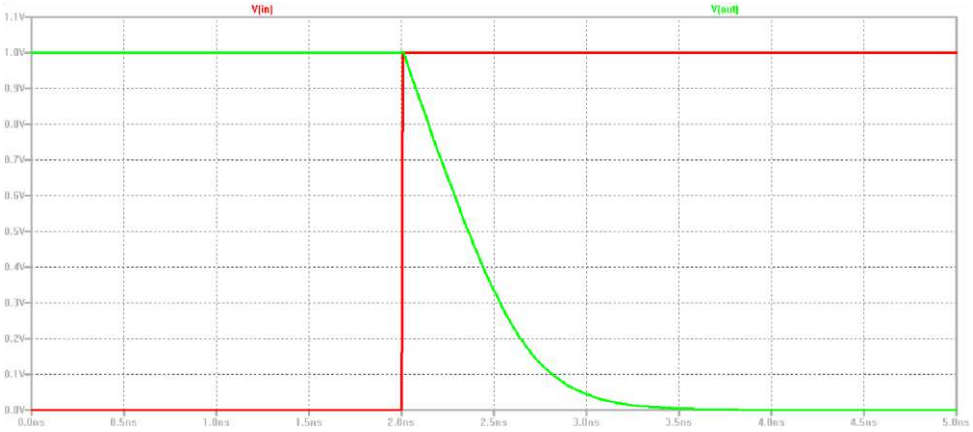


Figure 22: Transient Analysis plot for Digital Inverter

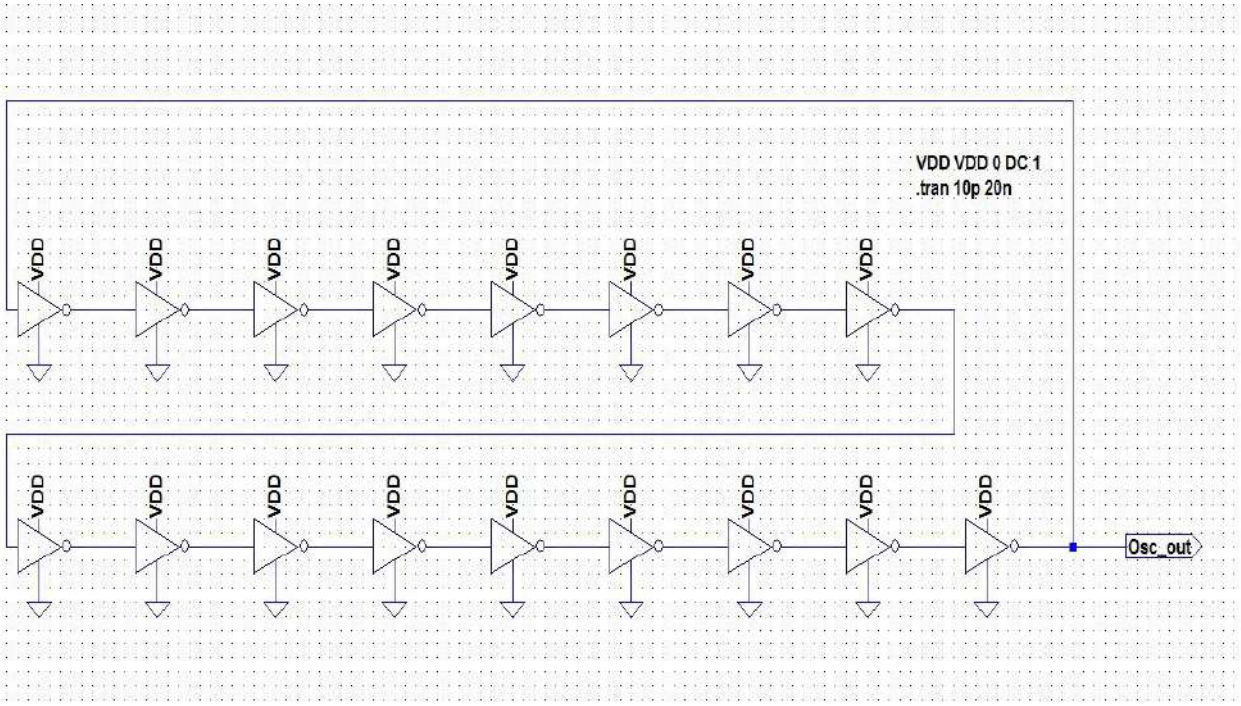


Figure 23: Schematic for Ring Oscillator

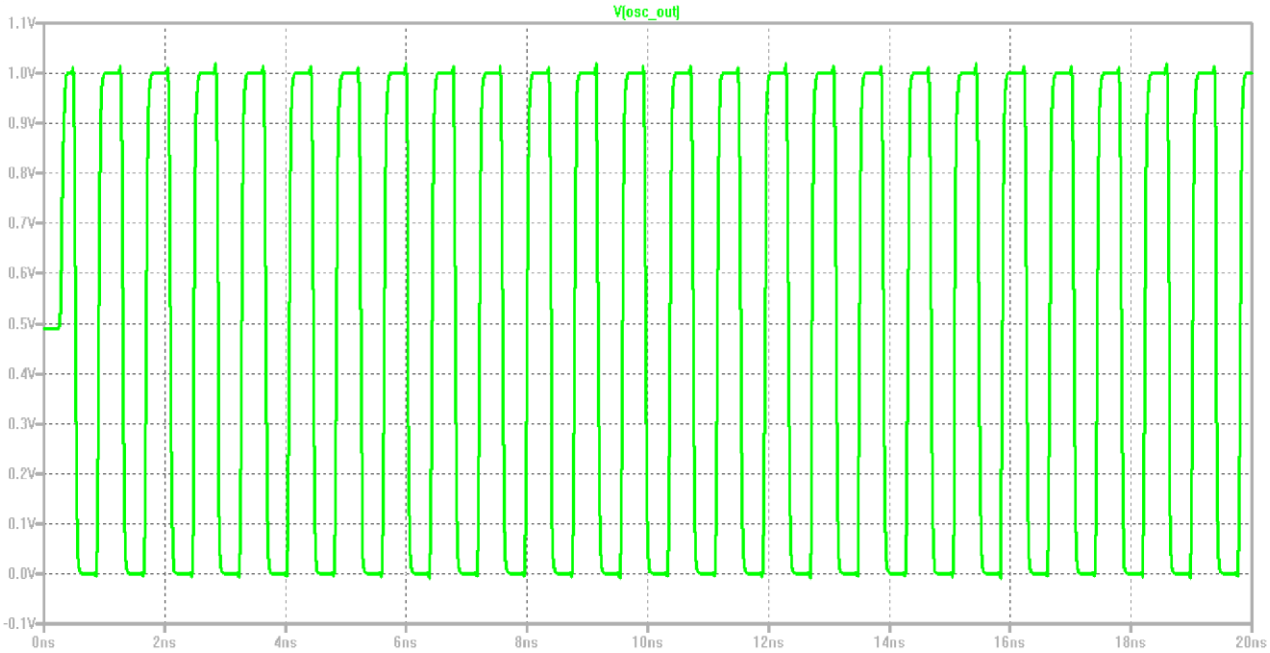


Figure 23: Transient plot for Ring Oscillator

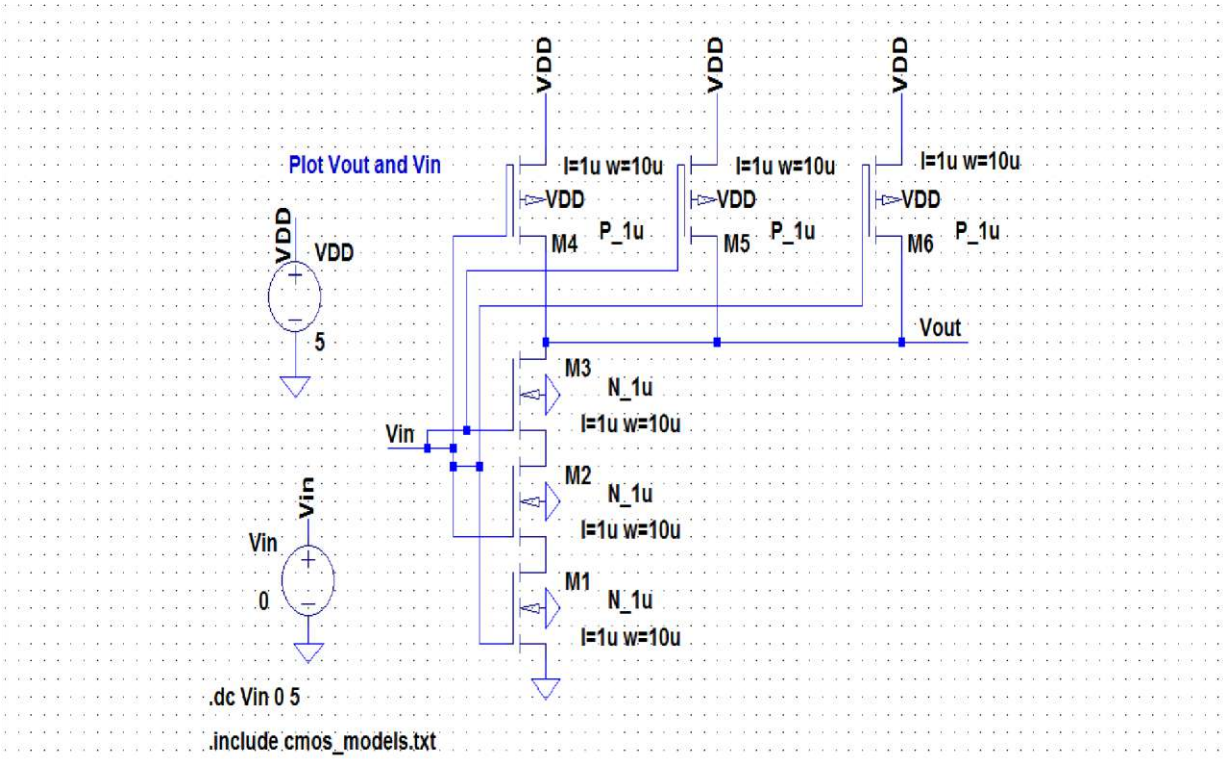


Figure 24: Schematic for 3 input NAND Gate

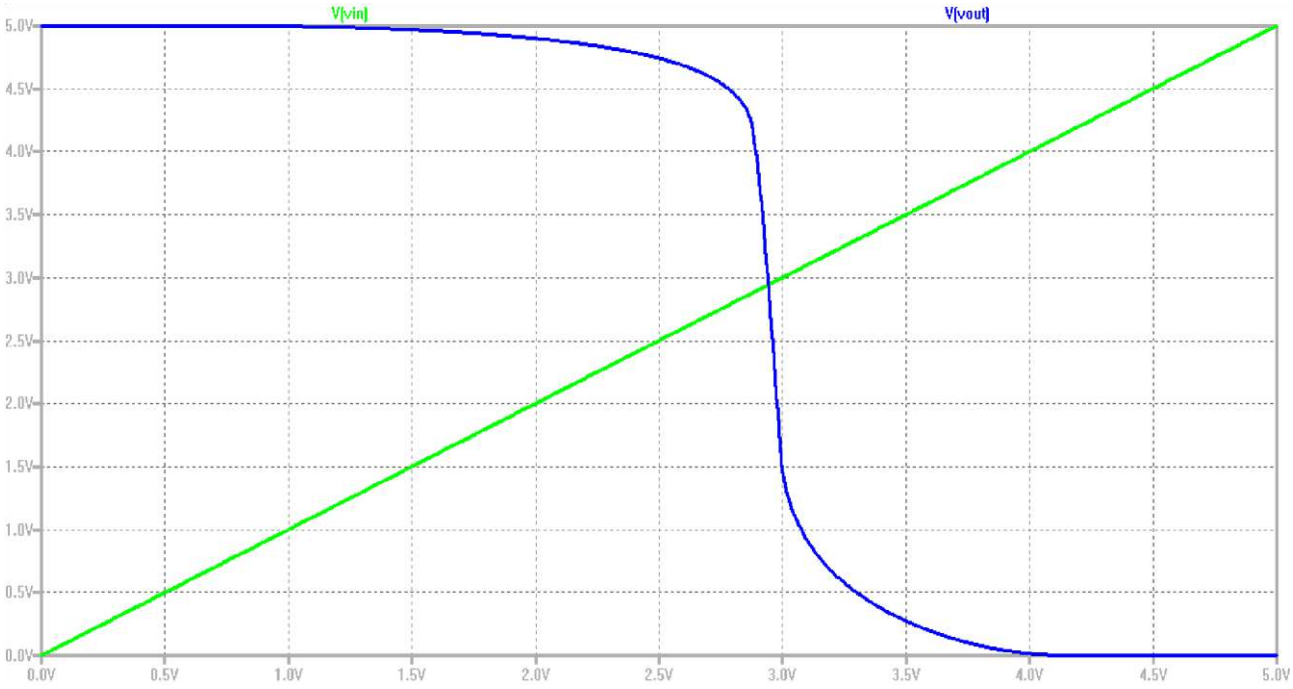


Figure 25: DC Analysis plot for 3 input NAND Gate

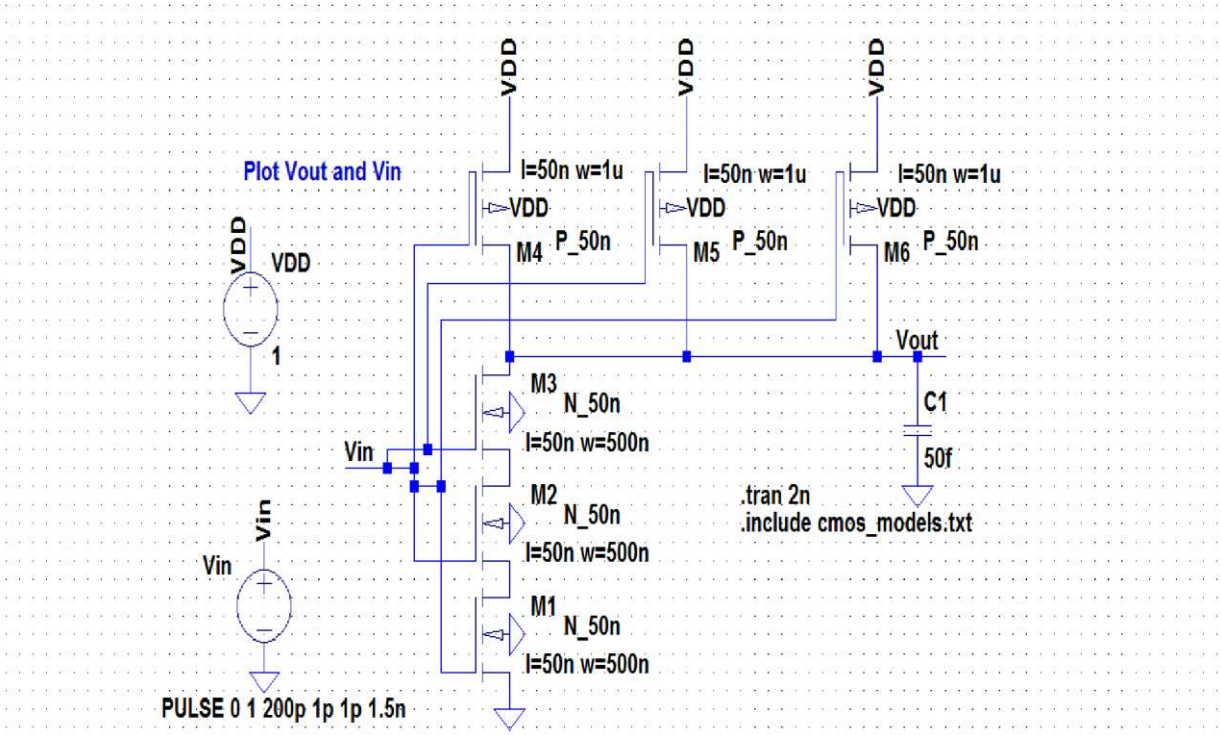


Figure 26: Schematic for 3 input NAND Gate

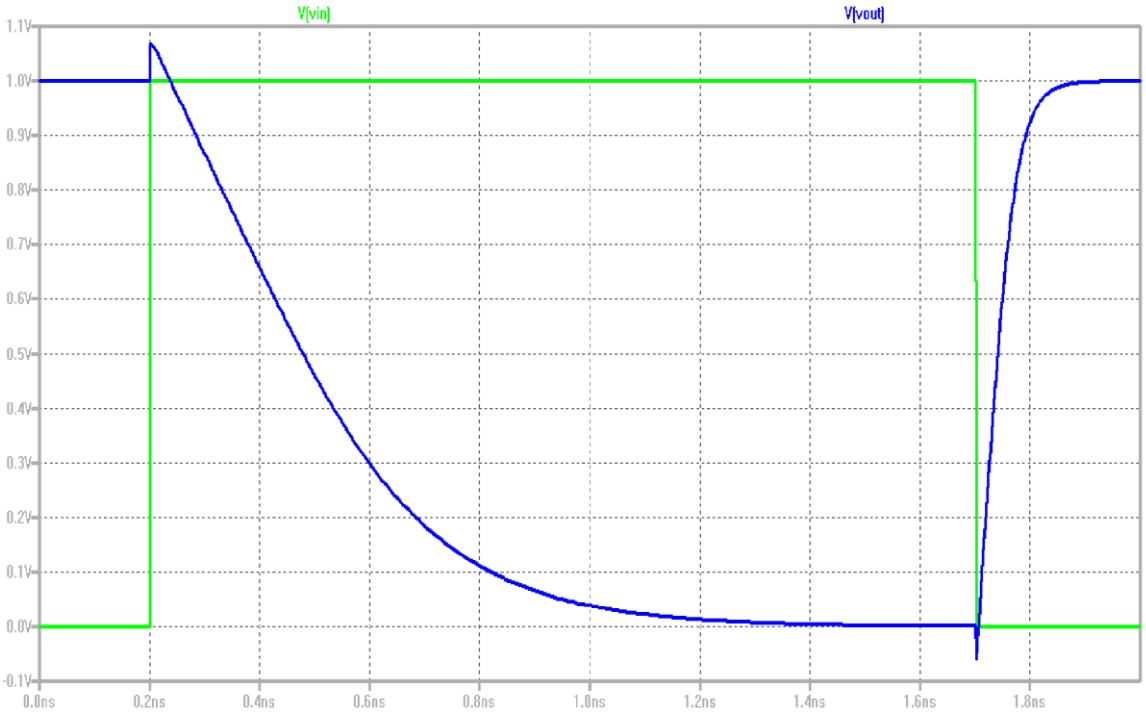


Figure 27: Transient plot for 3 input NAND Gate

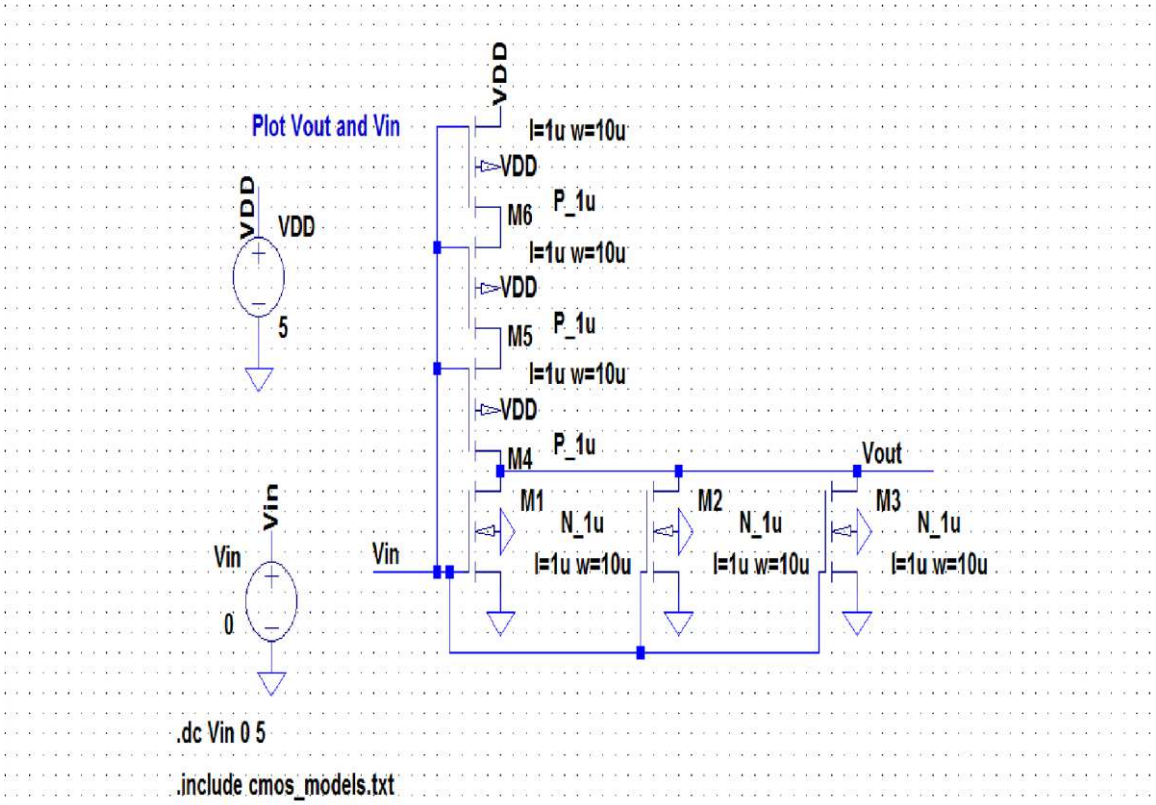


Figure 28: Schematic for 3 input NOR Gate

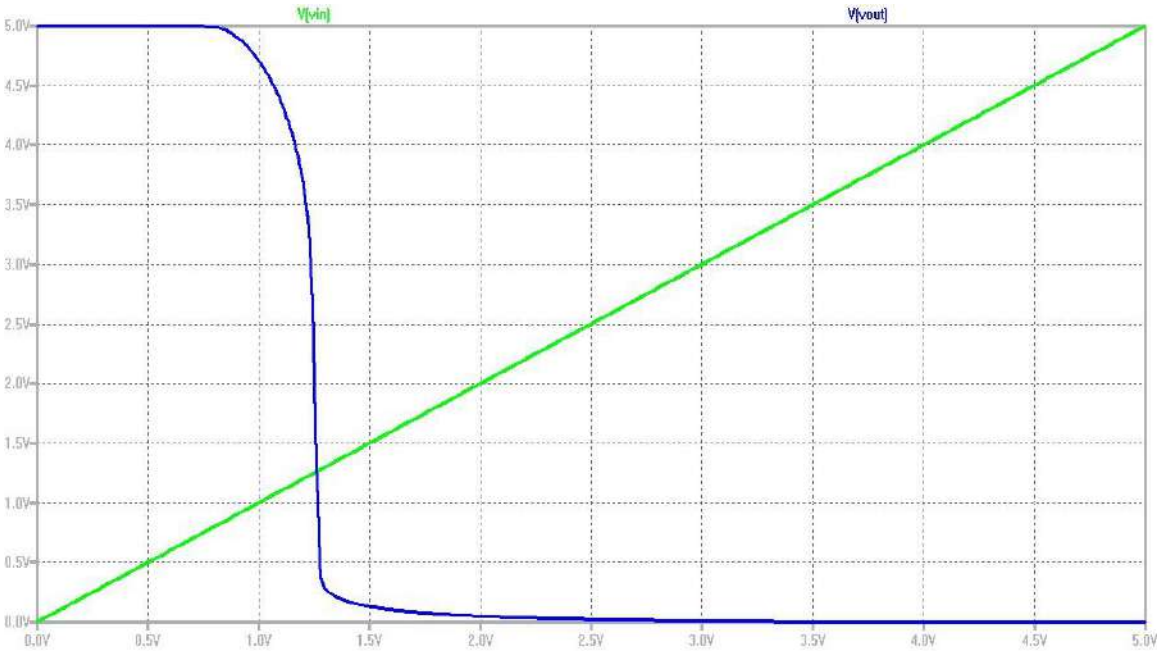


Figure 29: DC analysis plot for 3 input NAND Gate

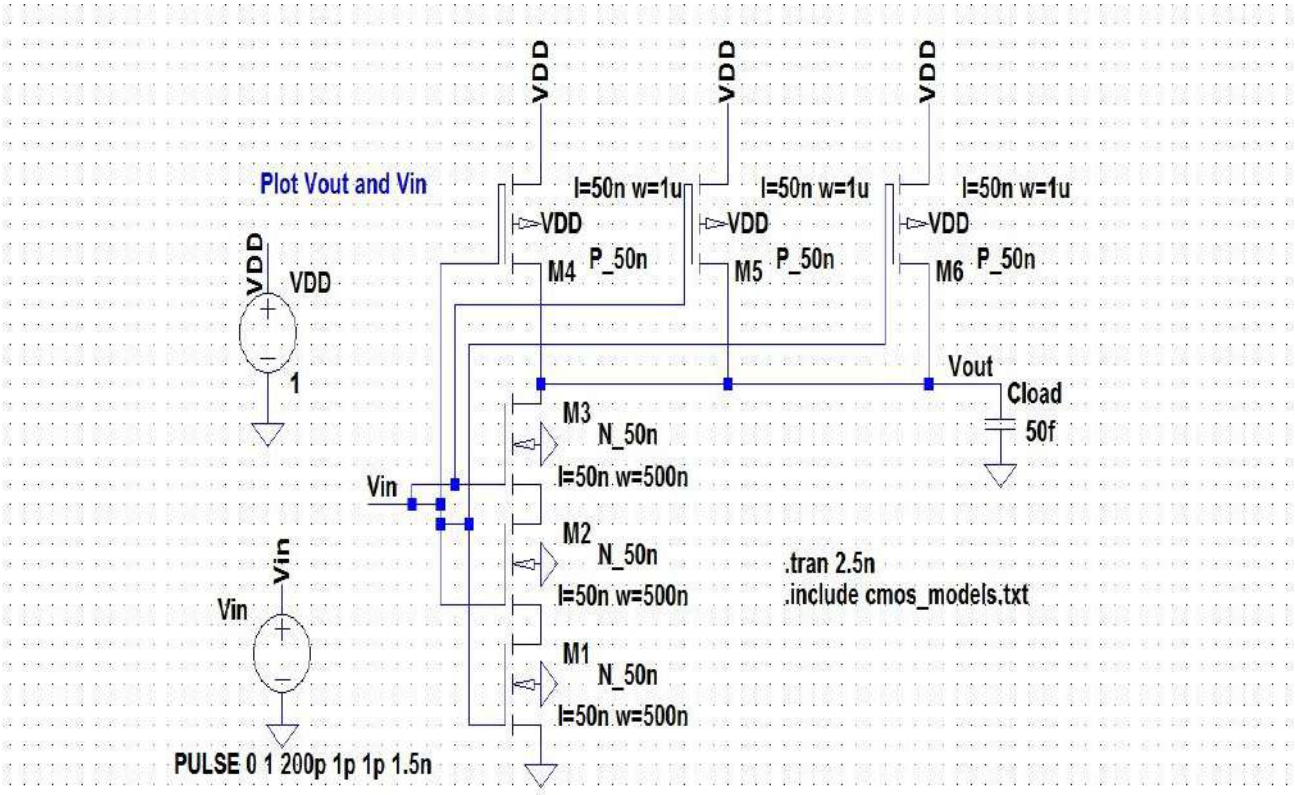


Figure 30: Schematic for 3 input NOR Gate

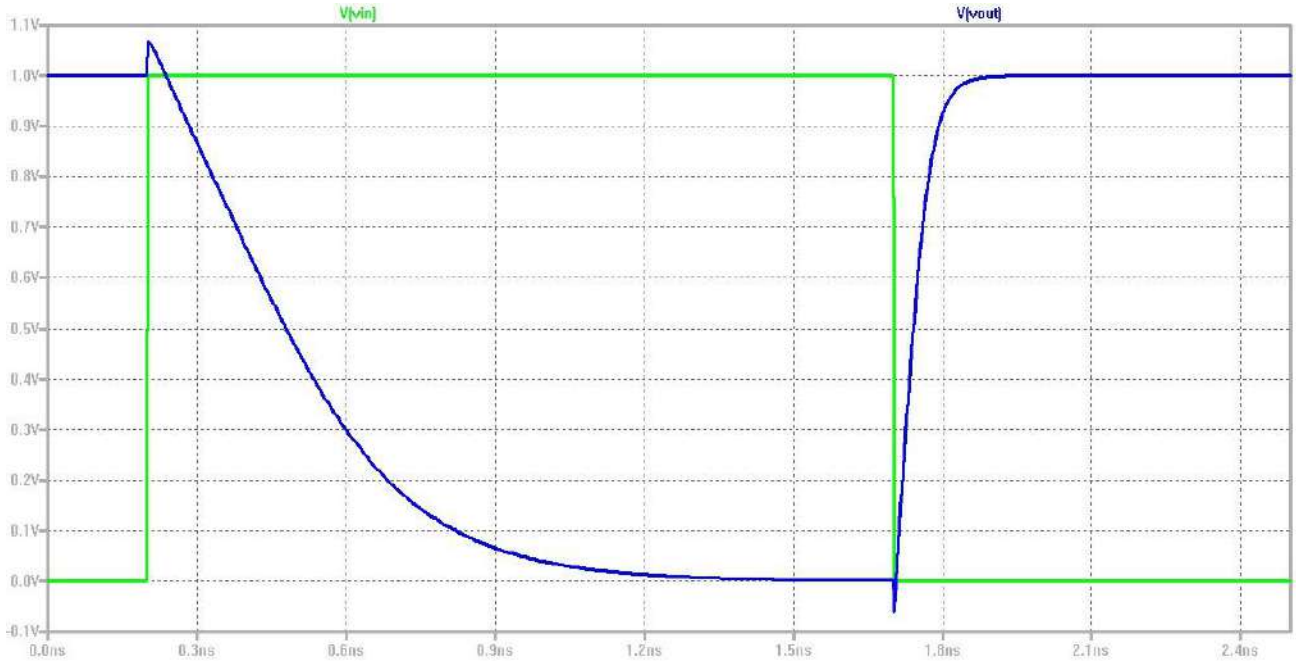


Figure 31: Transient plot for 3 input NOR Gate

Conclusion / Summary :

1. An ideal Op-Amp and sub circuits were modeled and necessary analysis was also done.
2. Following Simulation of MOS based circuits are also done using LTSpice

a. Inverter

b. Ring Oscillator

c. Gates

Viva Questions

1. What is an Operational Amplifier?
2. What is a Transconductor?
3. How Opamp can be used as
   a. Adder
   b. Substractor
   c. Integrator
   d. Differentiator

   Draw schematics to support your answer?
4. What is an Inverter?
5. How Inverter can be used as buffer?
6. What is Ring Oscillator?
7. What type of feedback is employed by ring oscillator?
8. Are the number of transistors used in Ring Oscillator even or Odd?
9. What is rise time, fall time and duty cycle?
10. What is a digital gate?

Experiment -4

Design Schematic, Layout and simulation of IV curves of PMOS and NMOS

Aim/Objective :

Design Schematic, Layout and simulation of IV curves of PMOS and NMOS

Theory :

Each transistor consists of a stack of a conducting gate, an insulating layer of silicon dioxide and a semiconductor substrate (body or bulk).

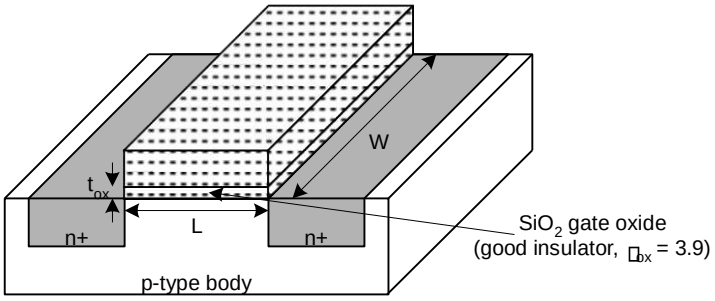


Figure 1: Basic MOS Transistor

nMOS transistor

2

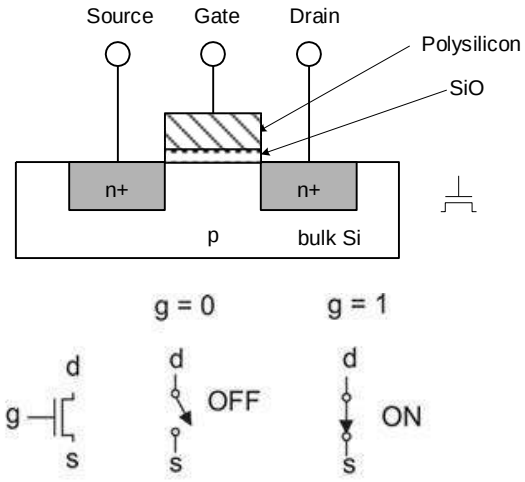


Figure 2 : NMOS structure, symbol and logic

4g=0: When the gate is at a low voltage ($V_{GS} < V_{TN}$):

- p-type body is at low voltage

- source and drain-junctions diodes are OFF
- transistor is OFF, no current flows

g=1: When the gate is at a high voltage ($V_{GS} \geq V_{TN}$):

- negative charge attracted to body
- inverts a channel under gate to n-type
- transistor ON, current flows, transistor can be viewed as a resistor

pMOS transistor

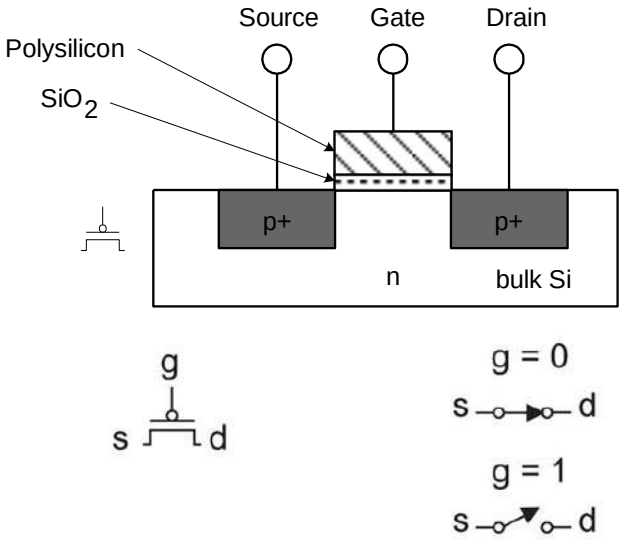


Figure 3: PMOS structure, symbol and logic

g=0: When the gate is at a low voltage ($V_{GS} < V_{TP}$):

- positive charge attracted to body
- inverts a channel under gate to p-type
- transistor ON, current flows

g=1: When the gate is at a high voltage ($V_{GS} \geq V_{TP}$):

- negative charge attracted to body
- source and drain junctions are OFF
- transistor OFF, no current flows

In this lab simulations are performed using default and cmos_models that includes 300nm c5 process, 1u model and 50n model.

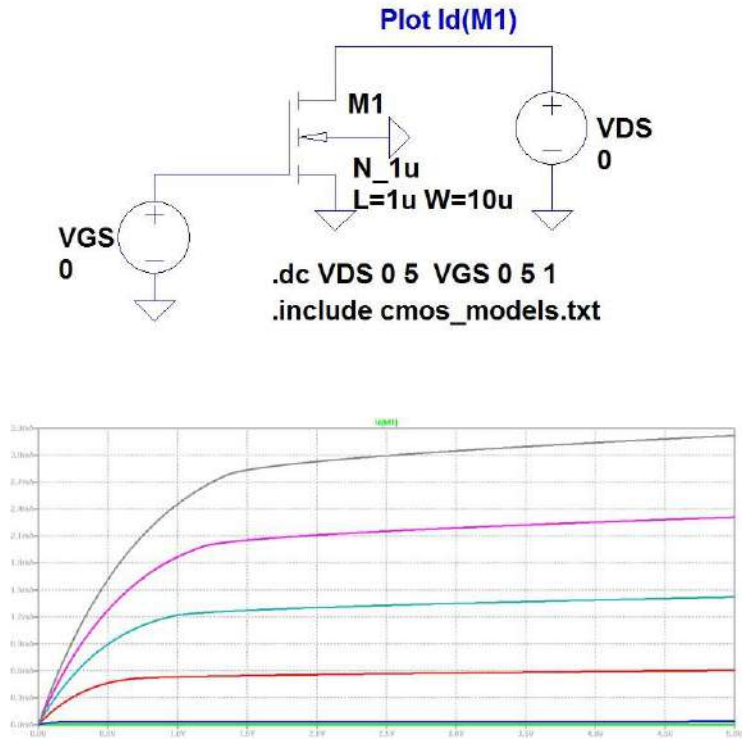


Figure 4: Schematic and plot for Id characteristics for NMOS 1u model

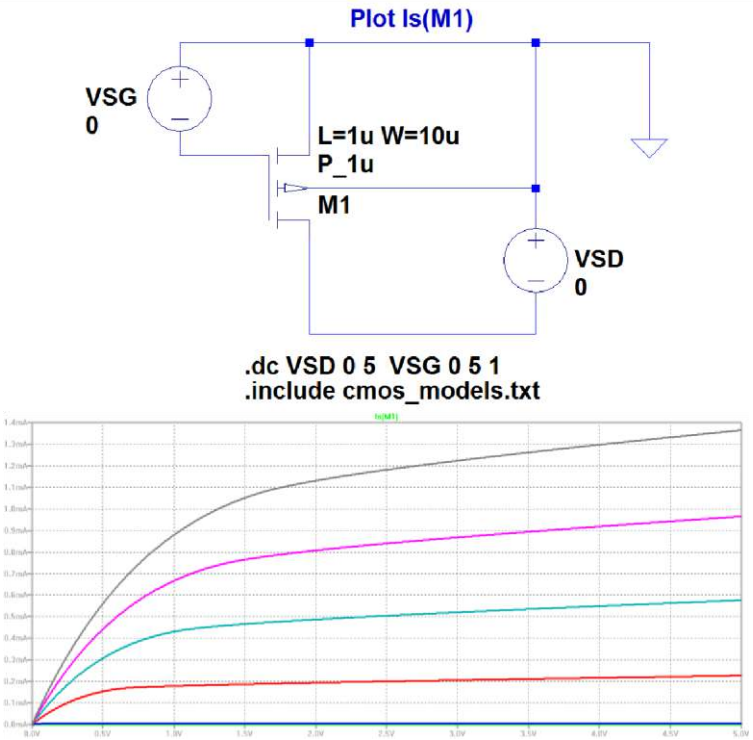


Figure 5: Schematic and plot for Is characteristics for PMOS 1u model

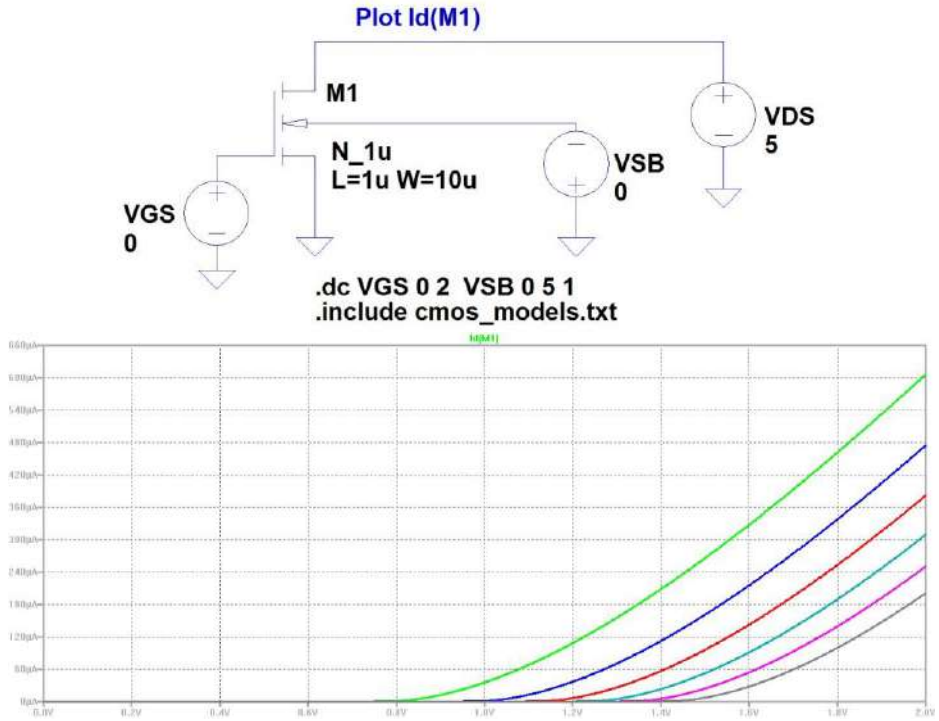


Figure 6: Schematic and plot for Id characteristics for NMOS 1u model

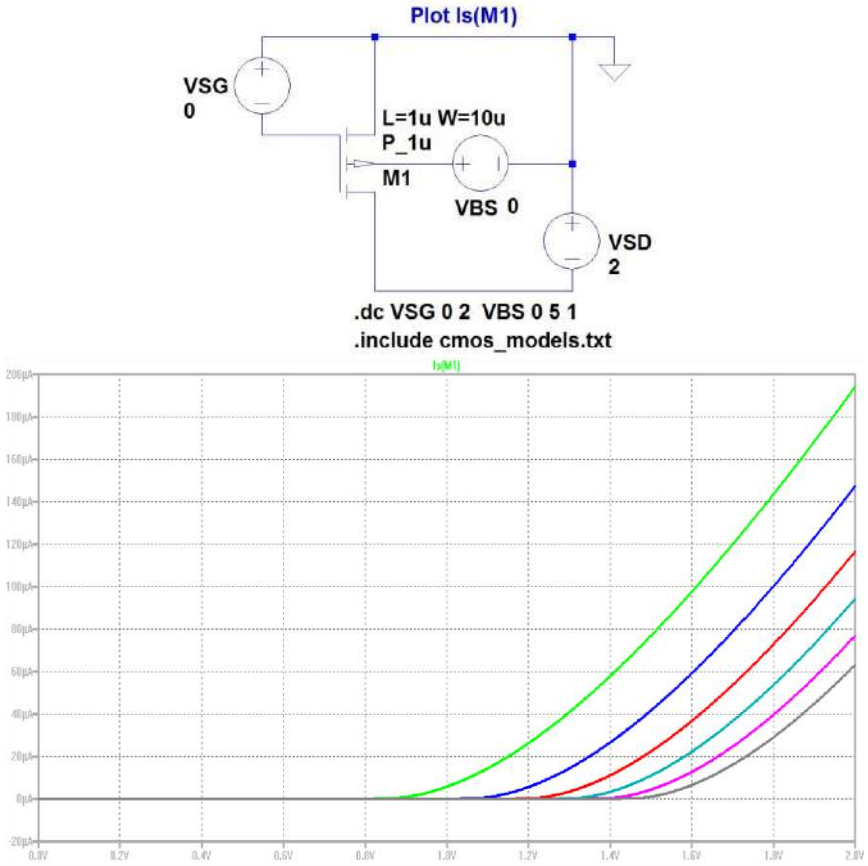


Figure 7: Schematic and plot for Is characteristics for PMOS 1u model

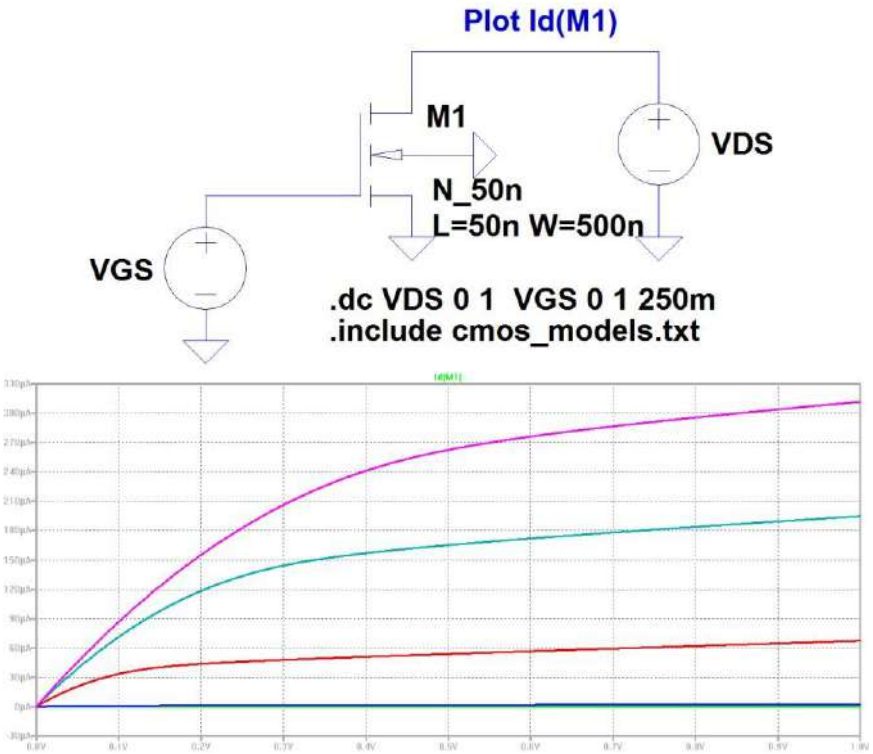


Figure 8: Schematic and plot for Id characteristics for NMOS 50n model

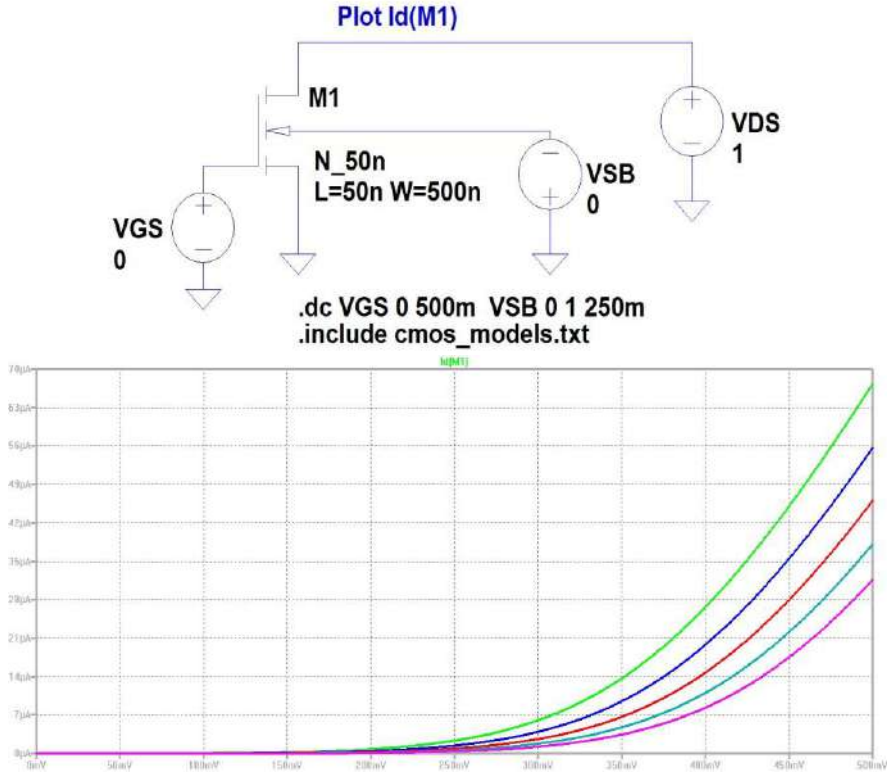


Figure 9:Schematic and plot for Id characteristics for NMOS 1u model

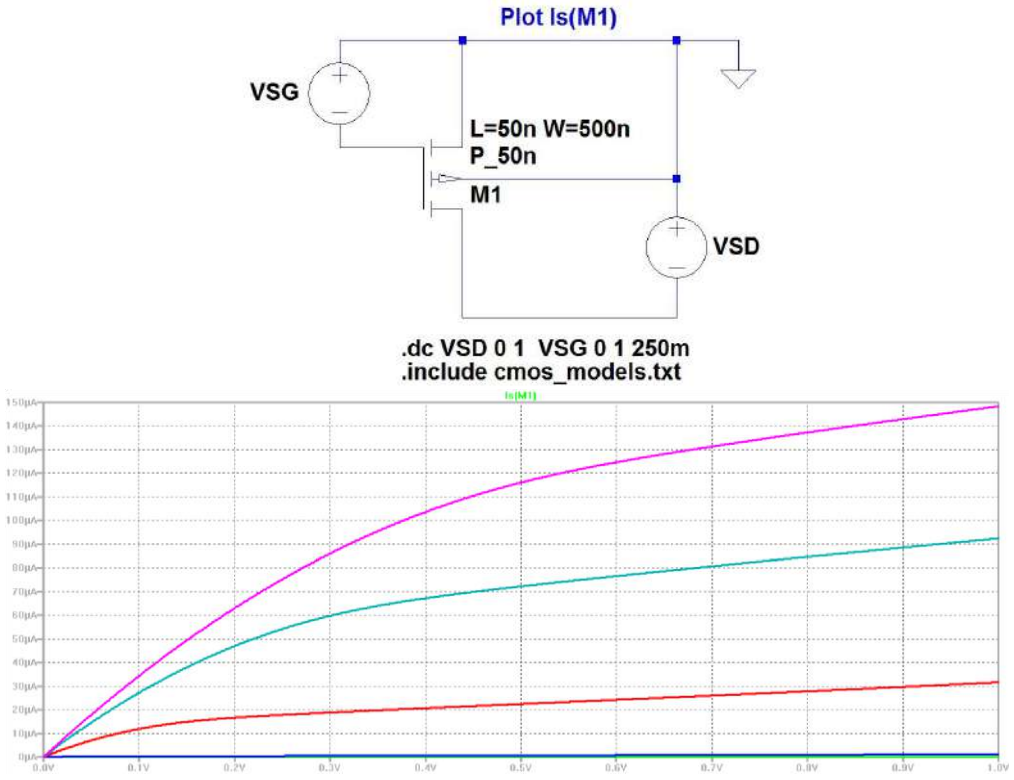
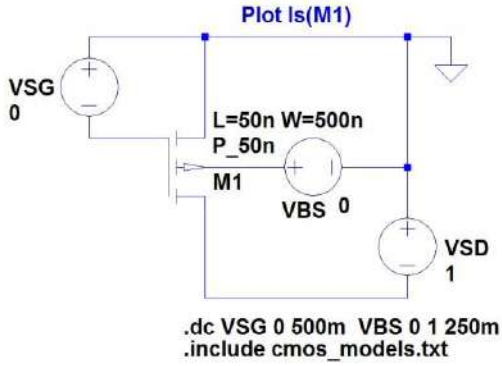


Figure 10: Schematic and plot for Is characteristics for PMOS 50n model



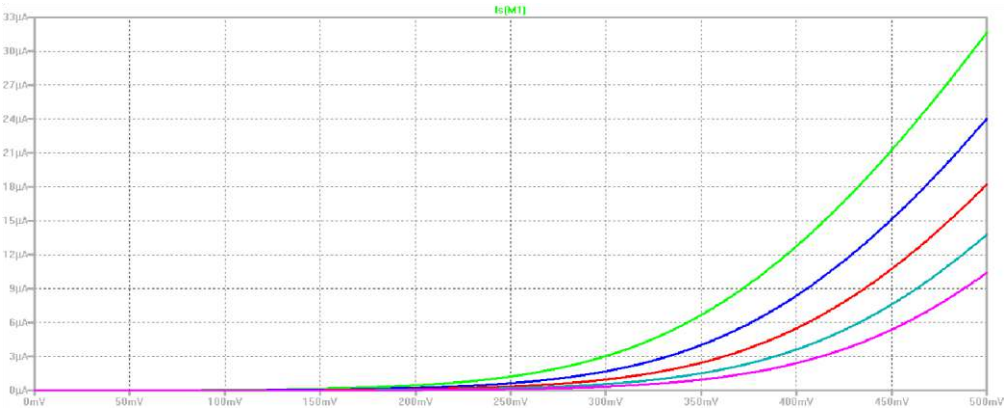


Figure 11: Schematic and plot for Is characteristics for PMOS 50n model

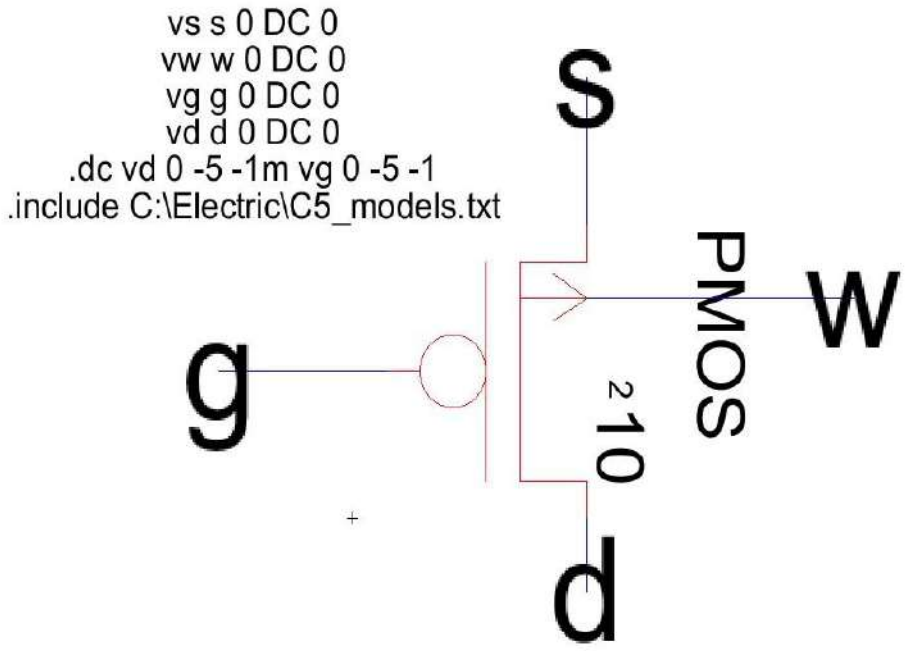


Figure 12: Schematic and spice code for DC characteristics for PMOS

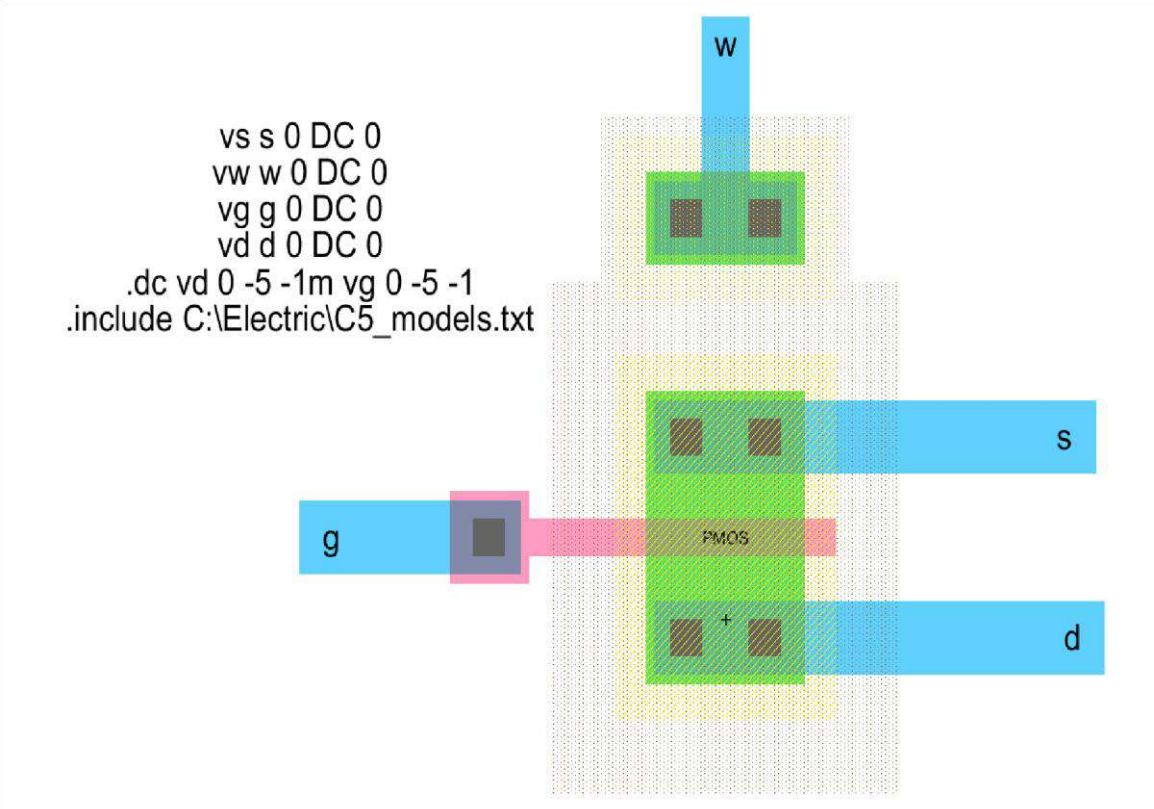
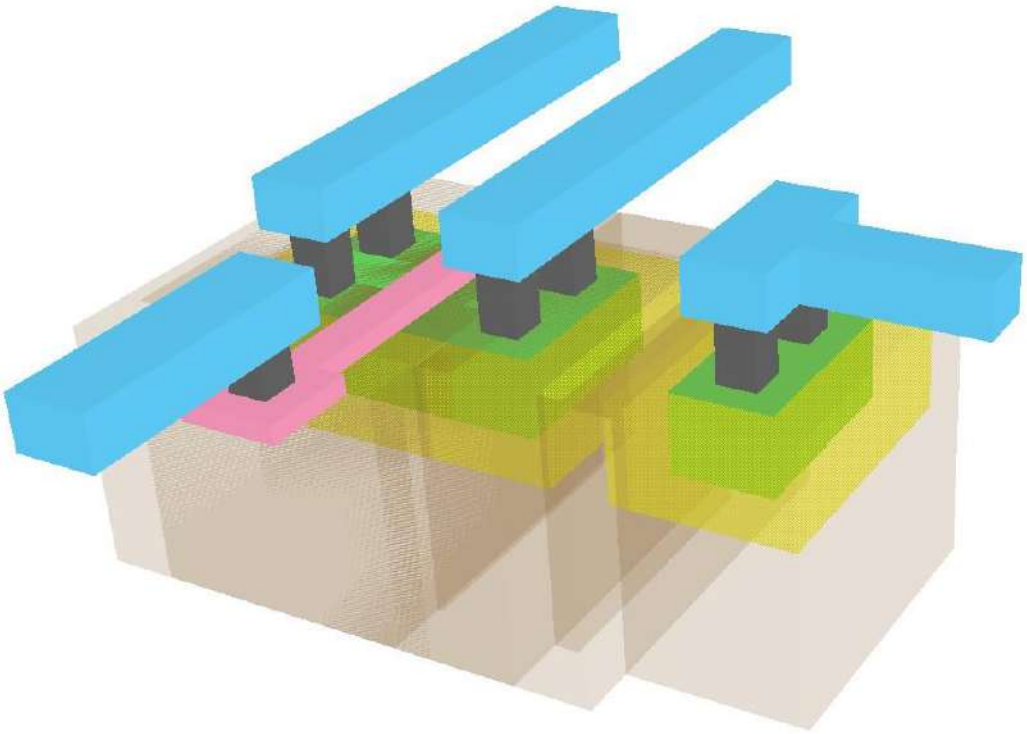


Figure 13: Layout and spice code for DC characteristics for PMOS



7

Figure 14: 3D view for PMOS Transistor

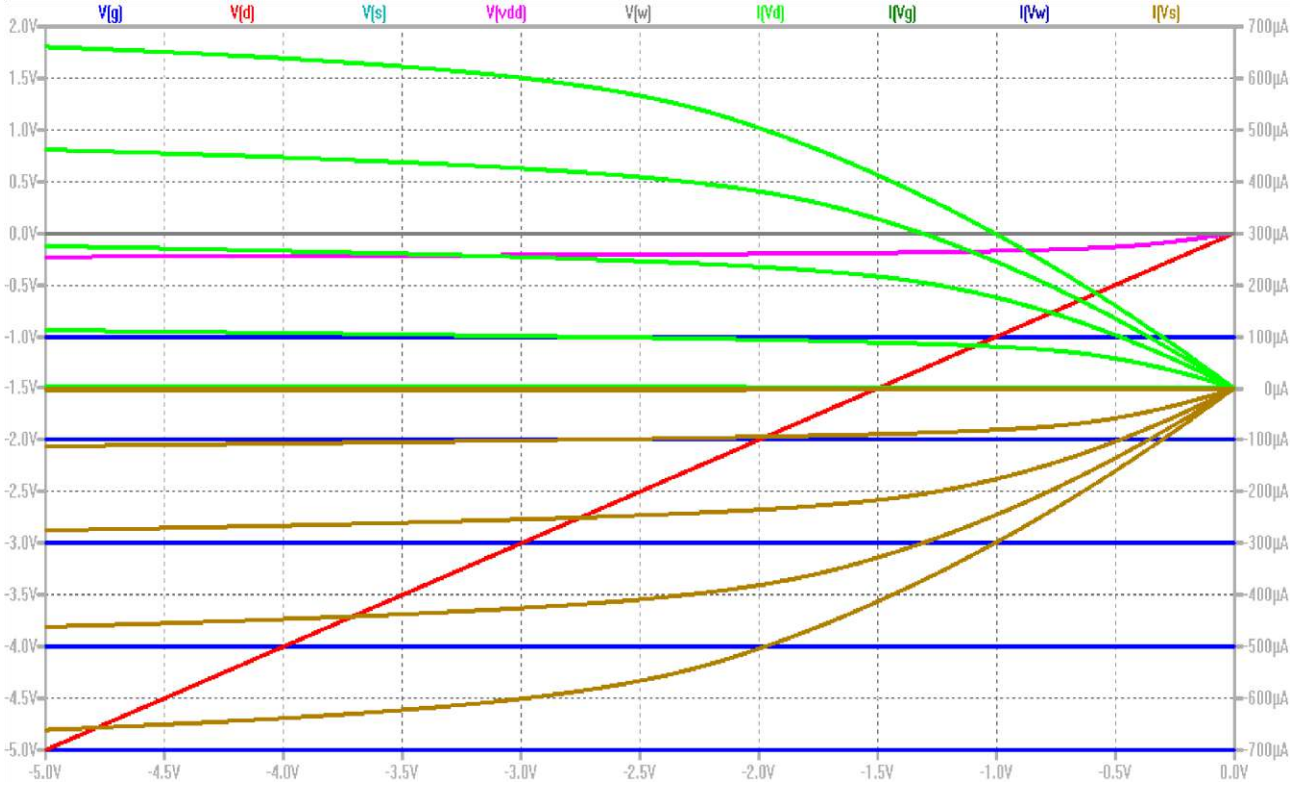


Figure 15: Simulation of various parameters for PMOS

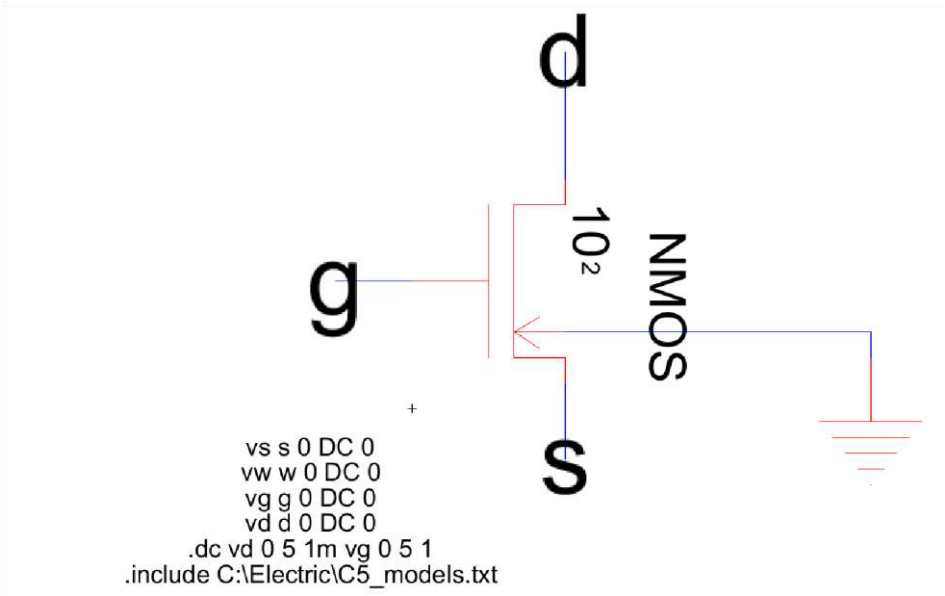


Figure 16: Schematic and spice code for DC characteristics for NMOS

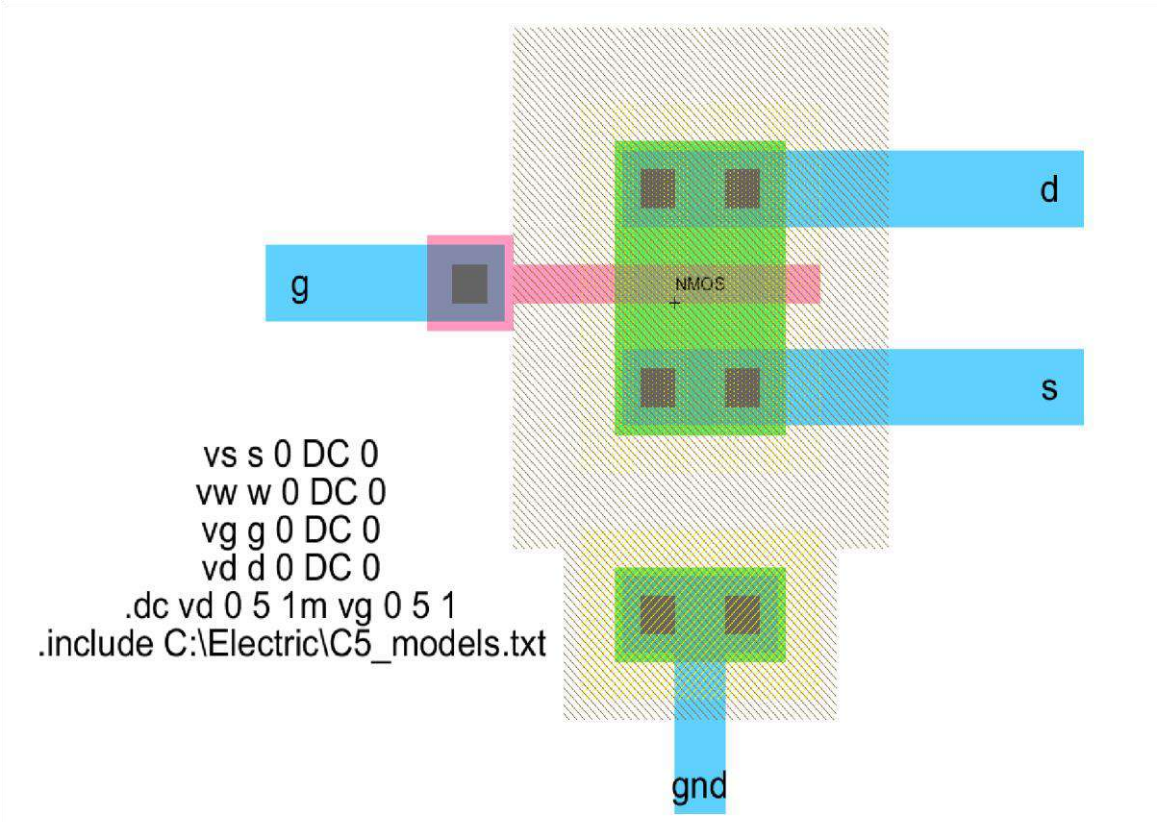


Figure 17: Layout and spice code for DC characteristics for NMOS

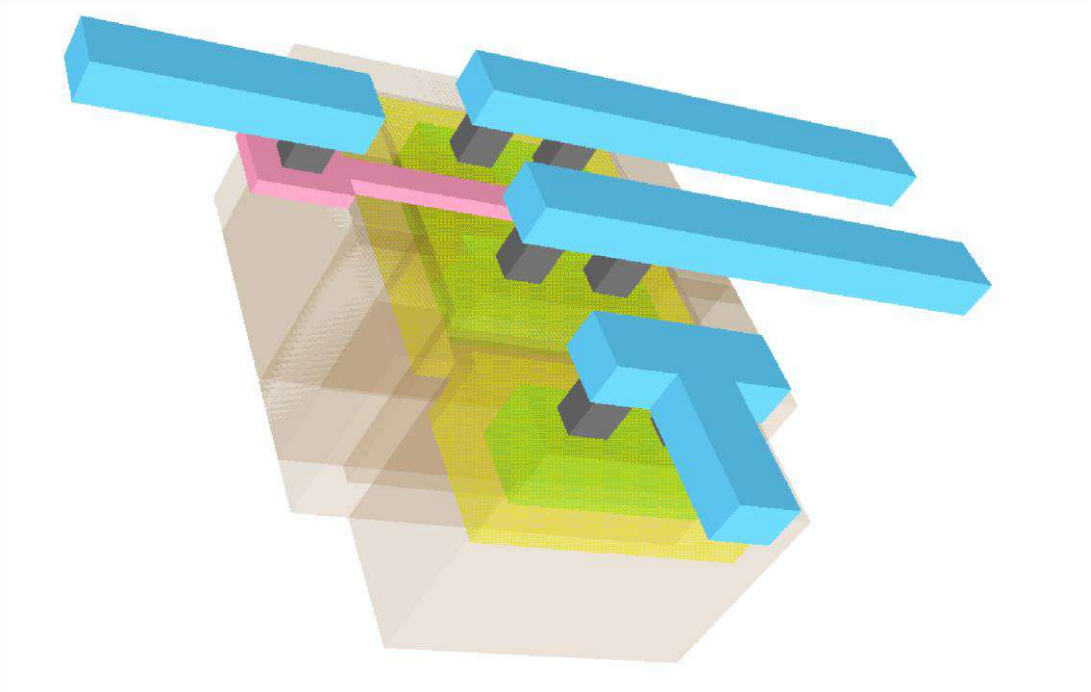


Figure 18: 3D view for NMOS Transistor

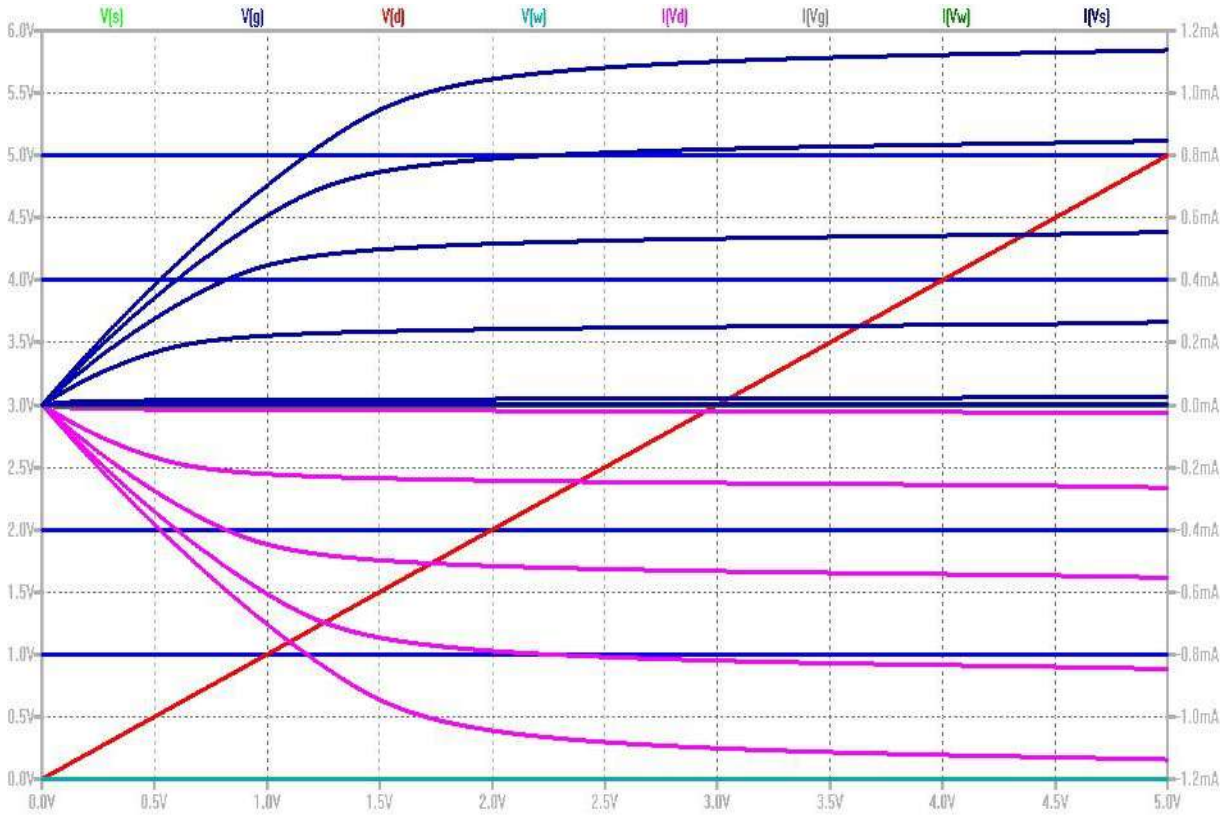


Figure 19: Simulation of various parameters for NMOS

Conclusion / Summary :

Design of Schematic and Layout and simulation and plotting of IV curves of PMOS and NMOS was done. Design was done using C5 process technology.

Viva Questions

1. What is a substrate or Unprocessed wafer ?
2. What is patterning ? how N-well and P-well are patterned ?
3. What are active and poly layers in layout design ?
4. What is standard cell frame ?
5. How is n+ different from n and P+ different from p ?
6. What are various design rules for NMOS and PMOS layout design ?
7. What is ESD (Electrostatic Discharge Protection)?
8. What is a Spice Model ?
9. Write the spice script used for PMOS IV Simulation ?
10. Write the spice script used for NMOS IV Simulation ?

Experiment -5

Design Schematic, Layout and simulation of CMOS Inverter

Aim/Objective :

Design Schematic, Layout and simulation of CMOS Inverter

Theory :

Each transistor consists of a stack of a conducting gate, an insulating layer of silicon dioxide and a semiconductor substrate (body or bulk). Here PMOS and NMOS are connected with gates and drain shorted to each other. Side view is shown in figure 2.

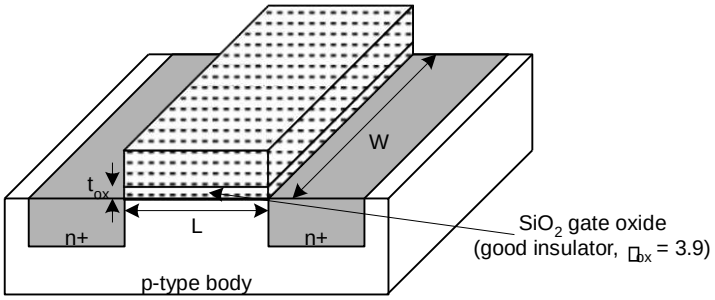


Figure 1: Basic MOS Transistor

The CMOS inverter is a basic building block for digital circuit design .As Figure 2 shows, the inverter performs the logic operation of A to Abar .When the input to the inverter is connected to ground, the output is pulled to VDD through the PMOS device M2 (and Ml shuts off). When the input terminal is connected to VDD, the output is pulled to ground through the NMOS device Ml (and M2 shuts off).The CMOS inverter has several important characteristics that are addressed in this lab: for example, its output Voltages wings from VDD to ground unlike other logic families that never quite reach the supply levels. Also, the static power dissipation of the CMOS inverter is practically zero, The inverter can be sized to give equal sourcing and sinking capabilities, and the logic Switching threshold can be set by changing the size of the device.

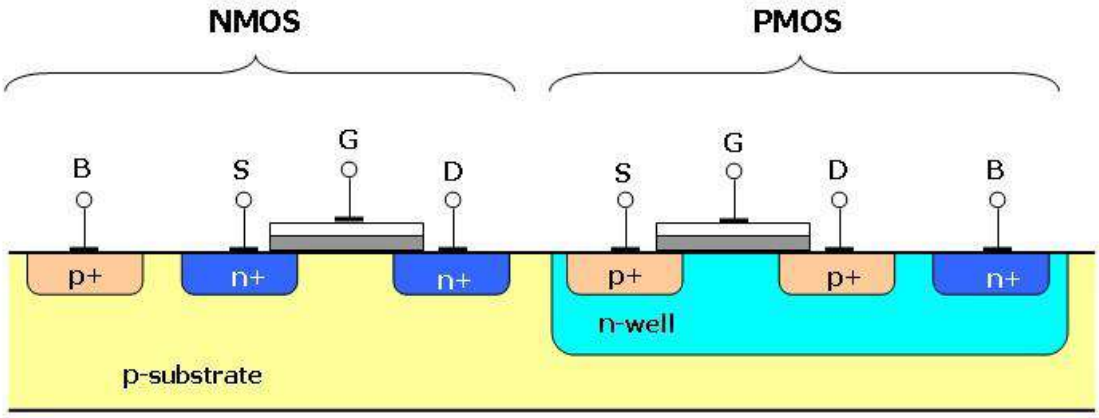


Figure 2 : Side view of CMOS Inverter

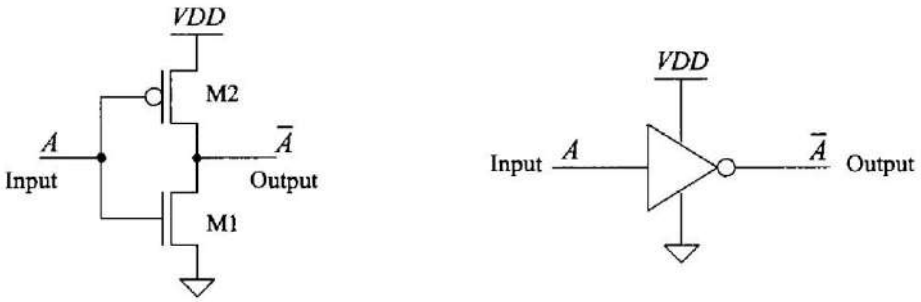


Figure 3: CMOS Inverter, schematic and logic symbol

As the inverter shown in Figure.4 and the associated transfer characteristic plot. In Region1of the transfer characteristics, the input voltage is sufficiently low (typically less than the threshold voltage of Ml), so that Ml is off and M2 is on (Vsa »VTHP). As Vin is increased, both M2 and Ml turn on (region2). Increasing Vin further causes M2 to turnoff and Ml to fully turn on, as shown in region3.

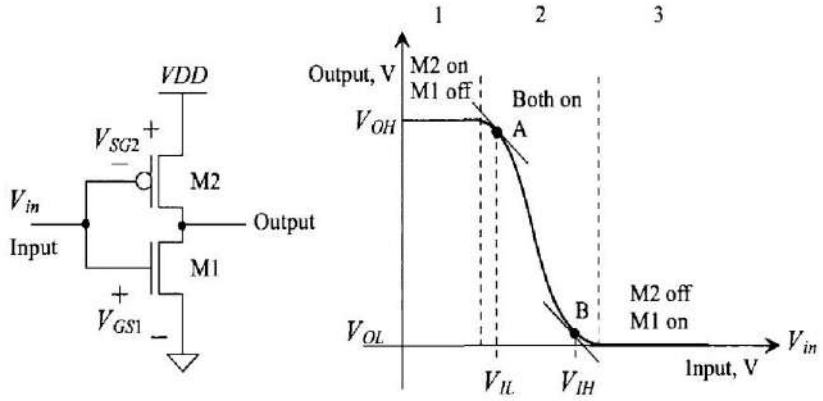


Figure 3: CMOS Inverter, DC transfer characteristics

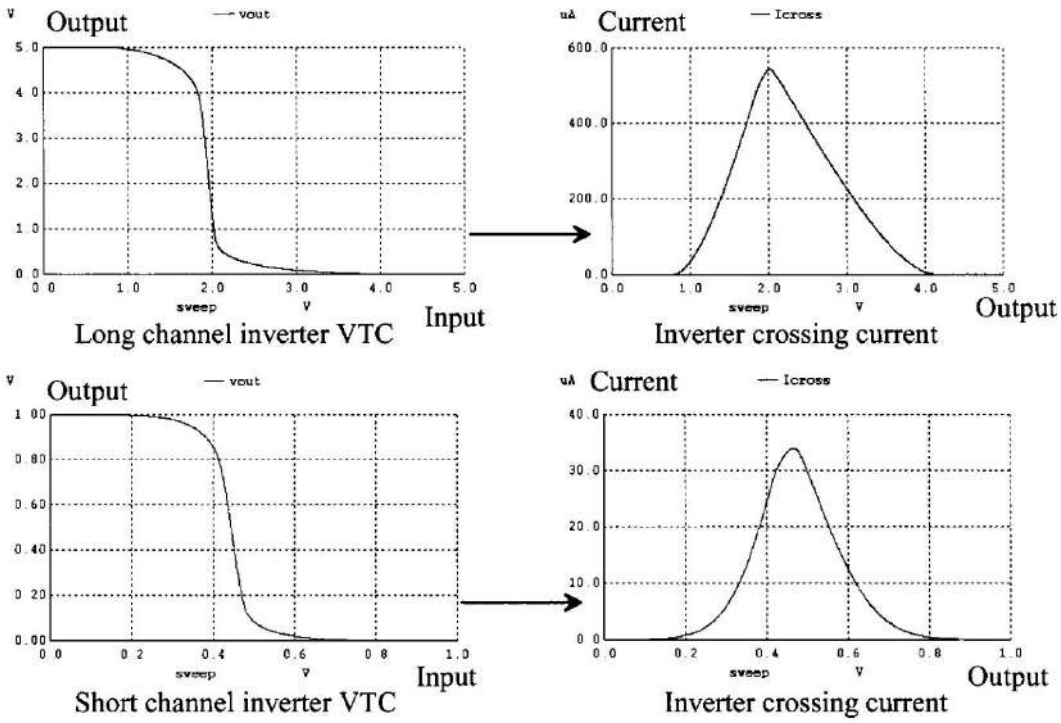


Figure 4: Voltage transfer curves (VTCs) for a long and a short channel inverter. In this lab simulations are performed using default and cmos_models that includes 300nm c5 process, 1u model and 50n model.

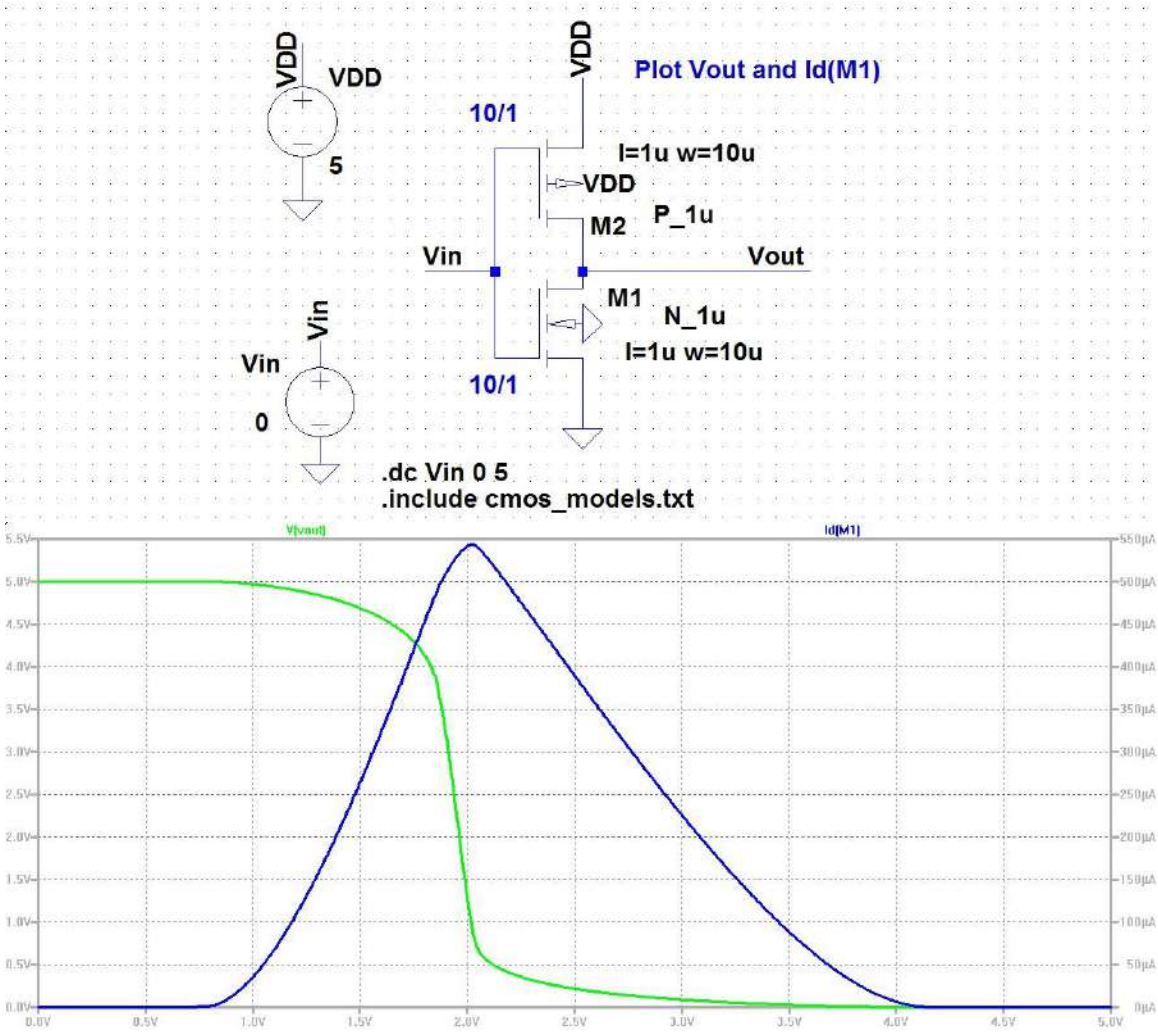
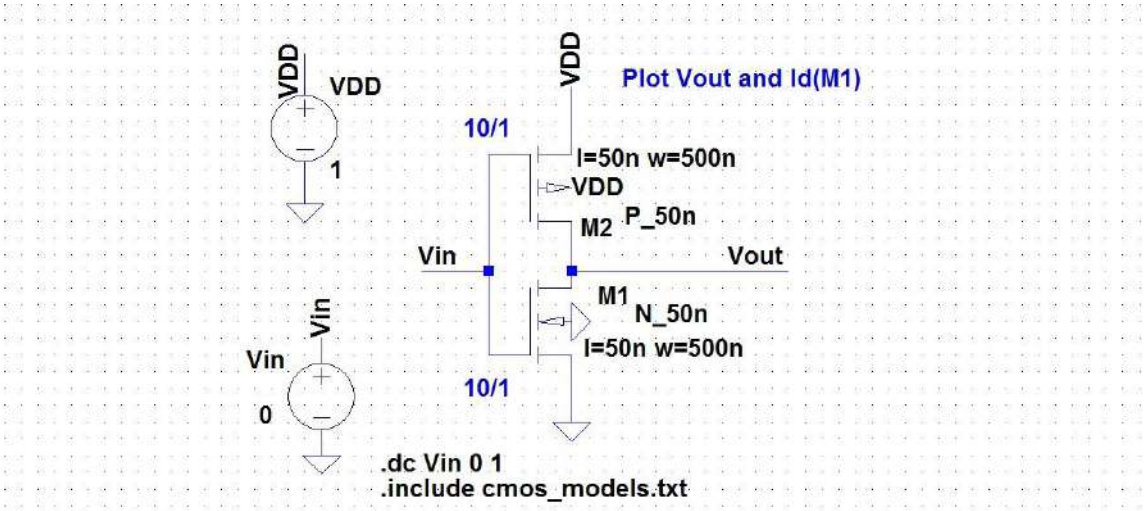


Figure 5: Voltage Current characteristics for a long channel inverter



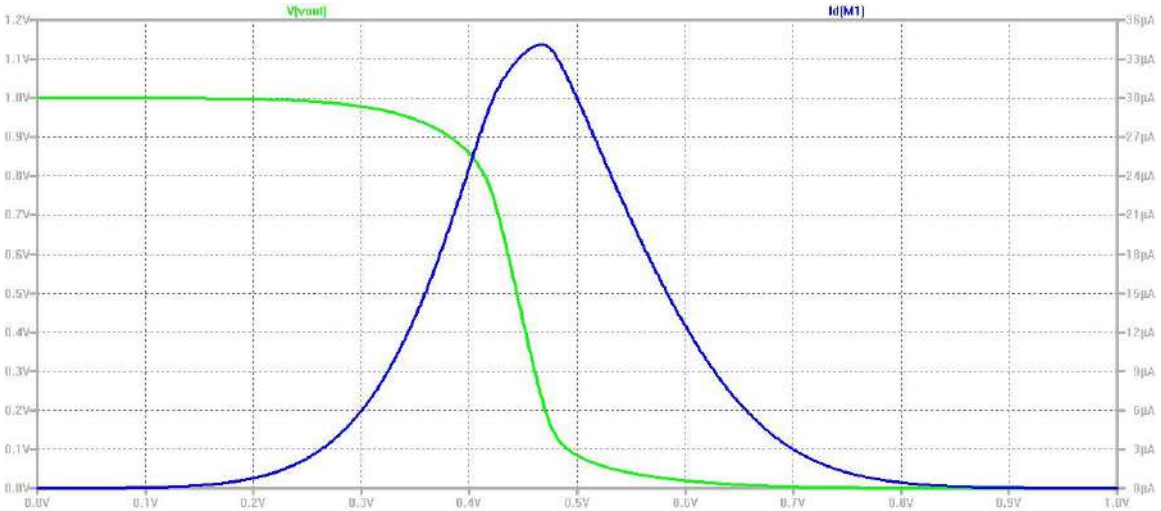


Figure 6: Voltage Current characteristics for a short channel inverter

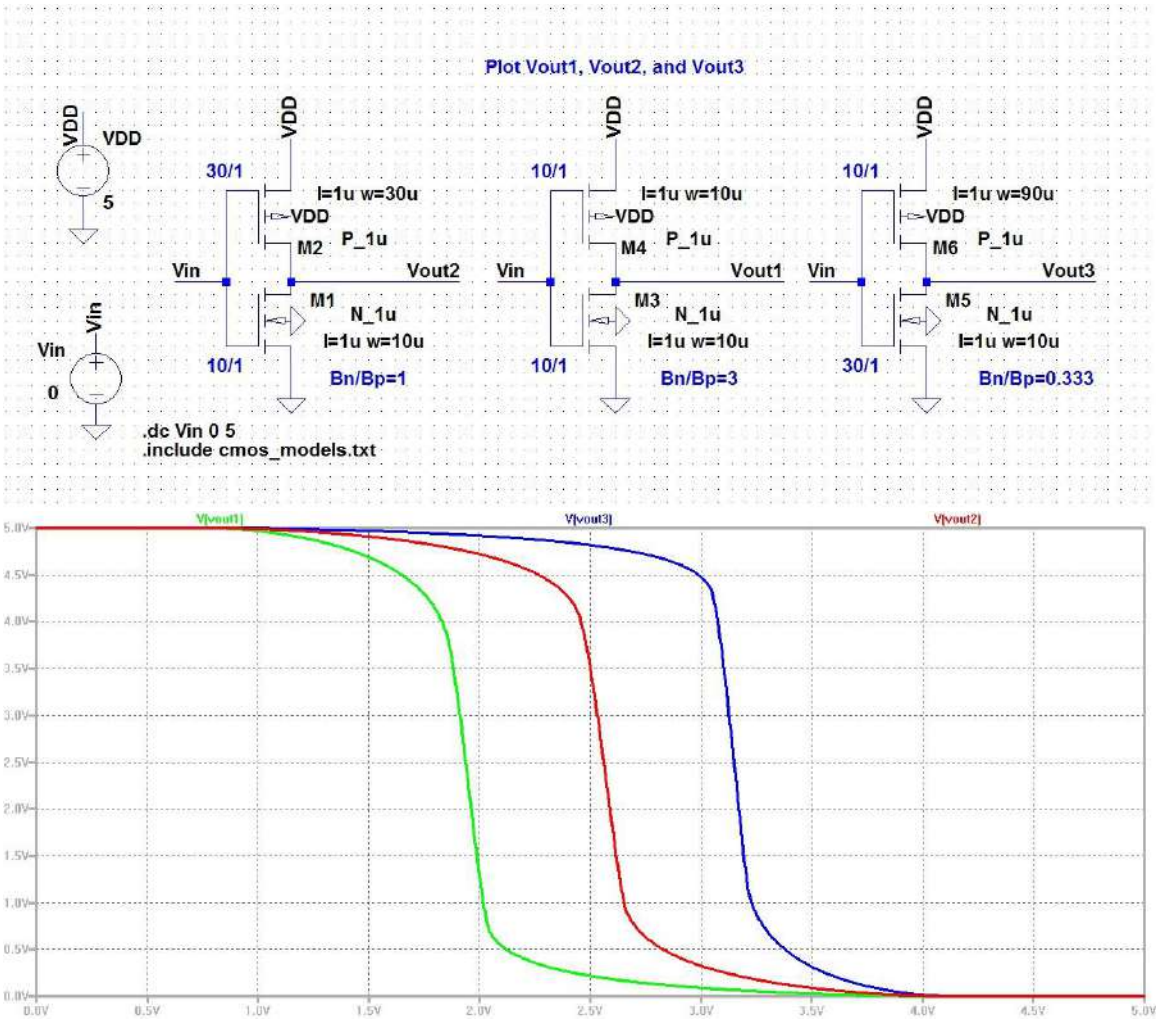
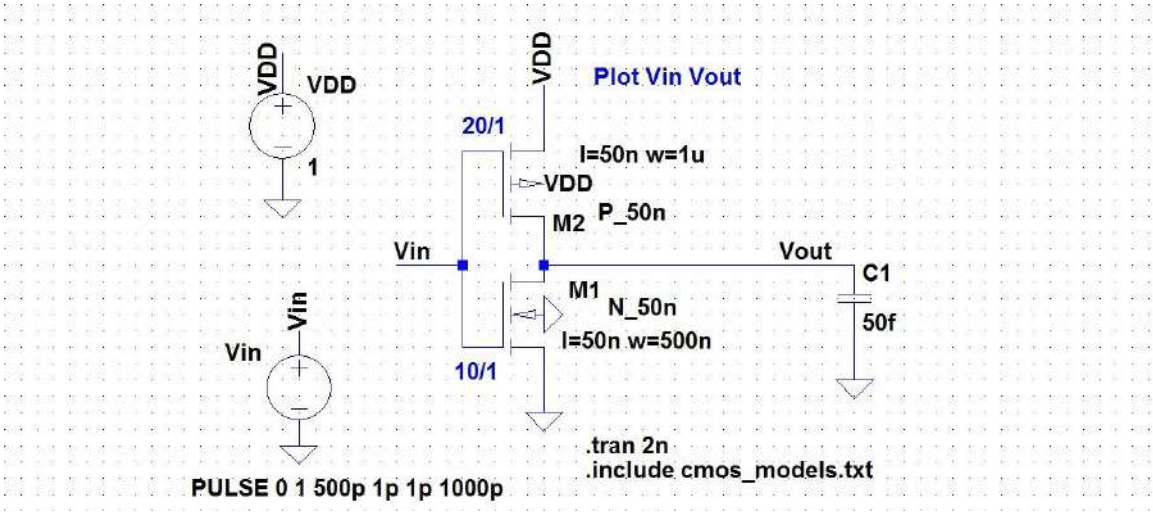


Figure 7: Voltage characteristics for different widths CMOS inverters



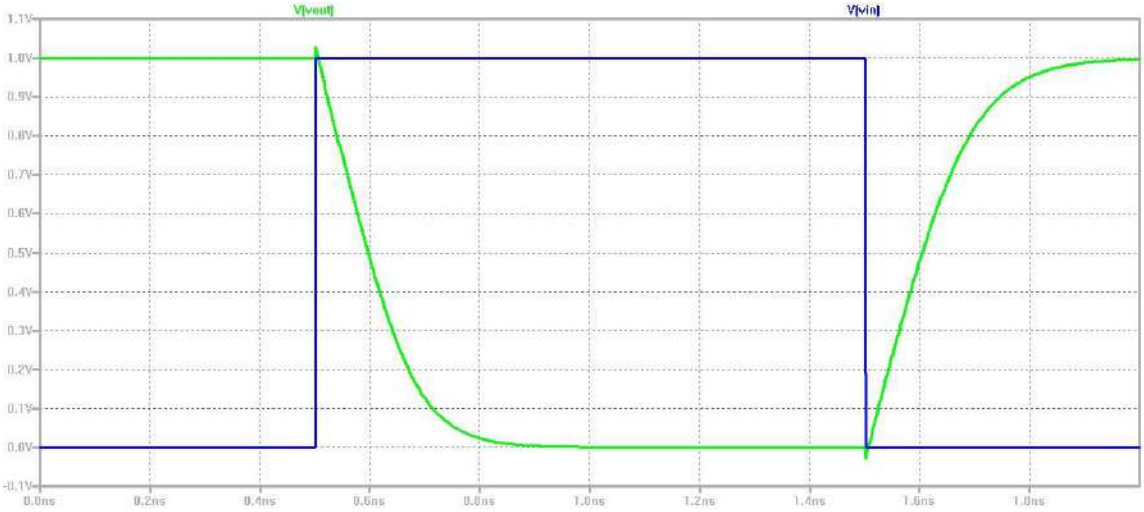
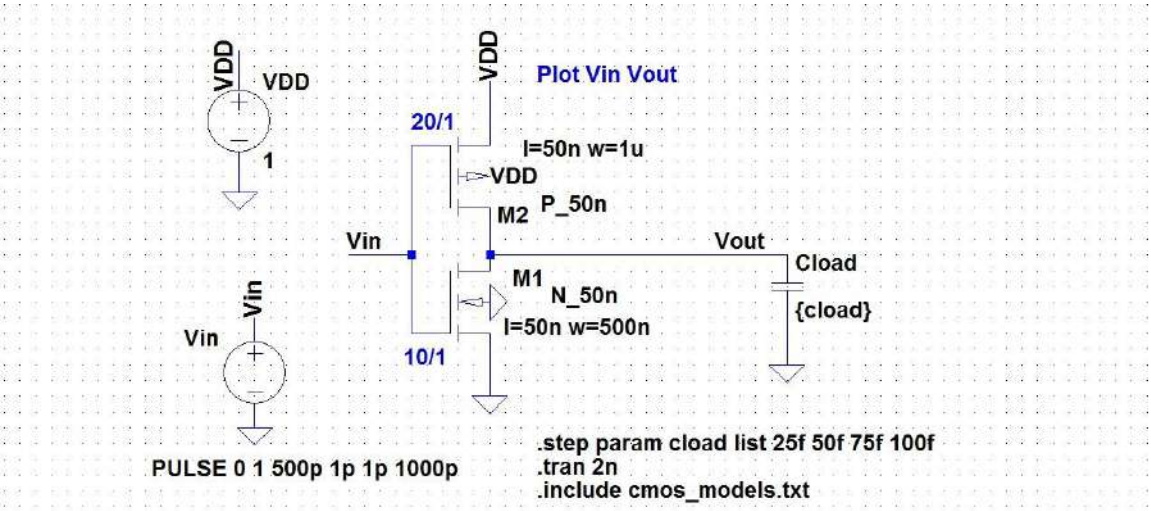


Figure 8: Voltage Transfer characteristics for CMOS inverter with varying load



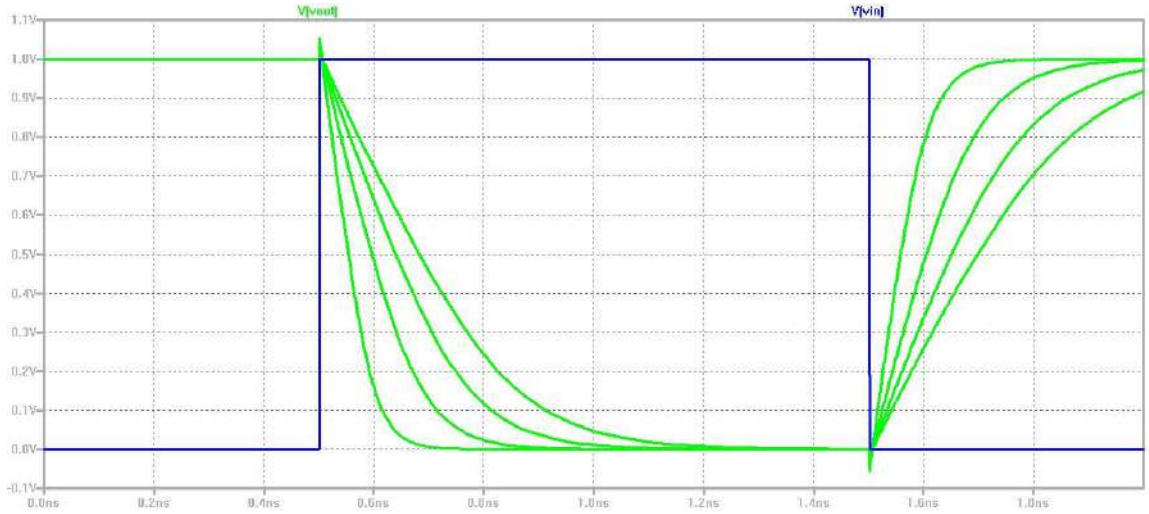


Figure 9: Voltage Transfer characteristics for CMOS inverter with varying load and pulsating input

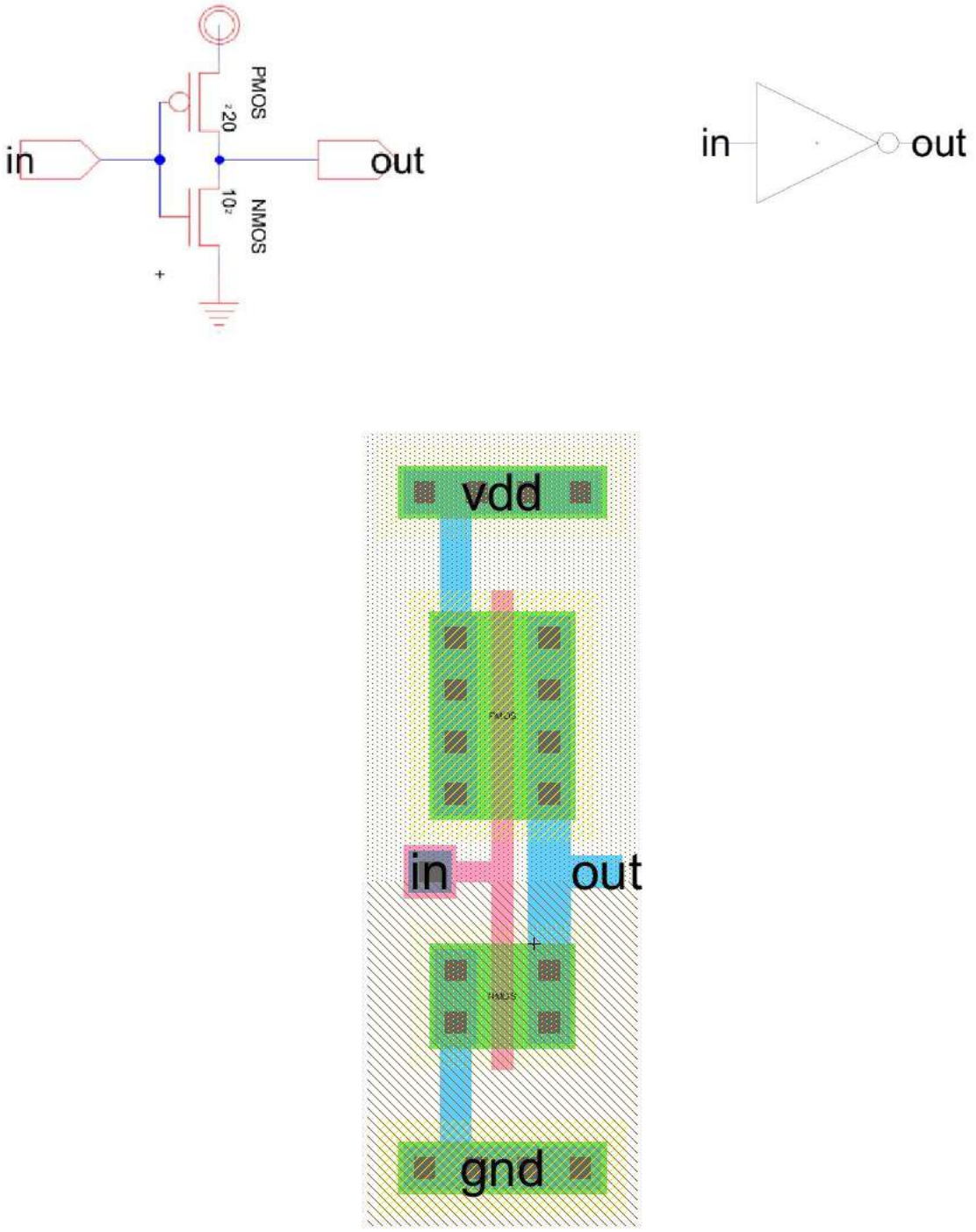
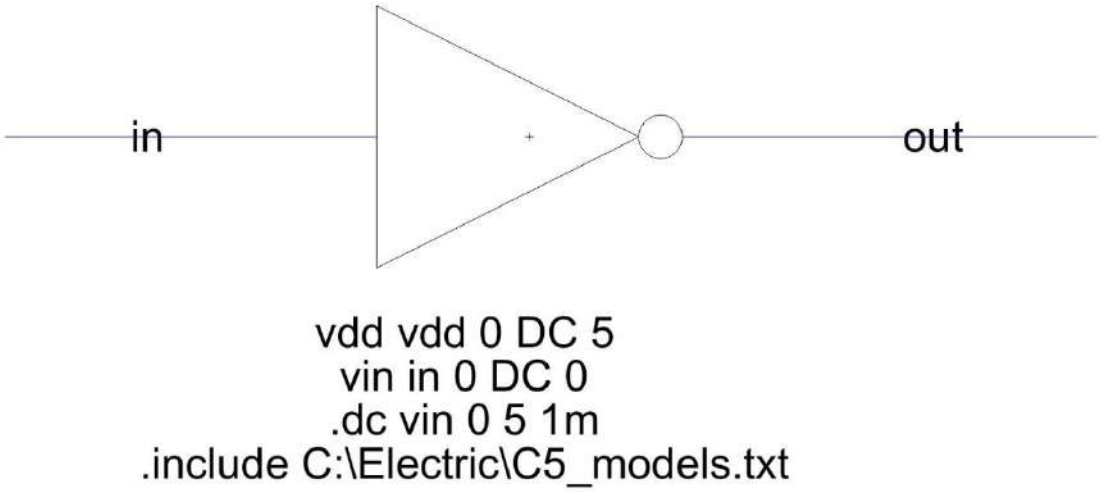


Figure 10:Schematic, icon and layout for CMOS Inverter



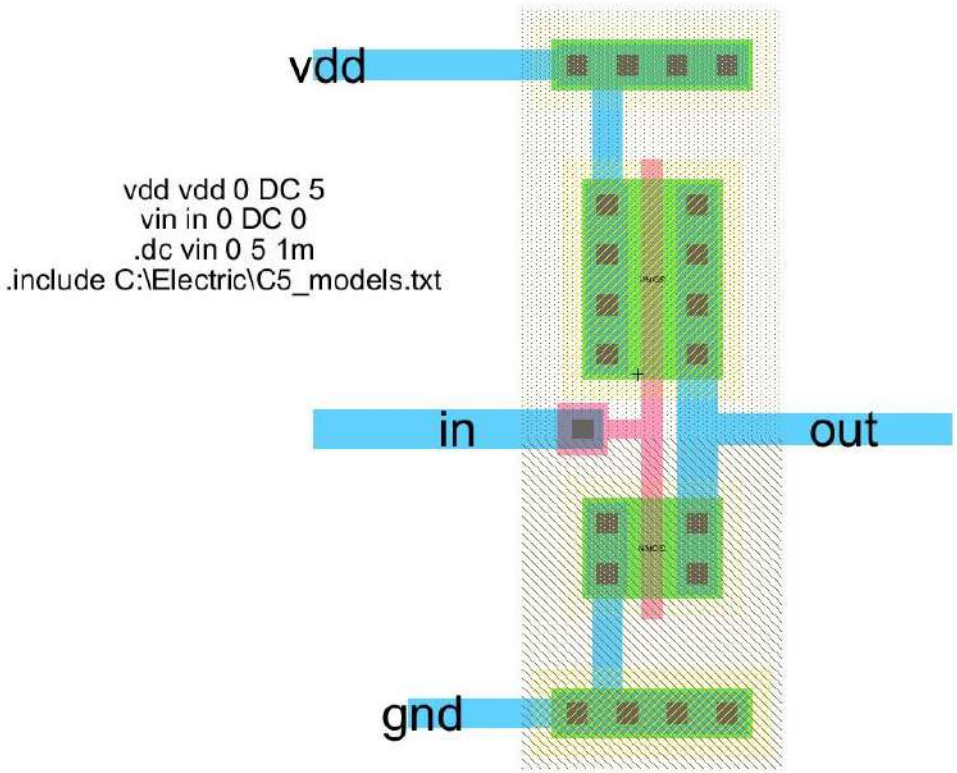


Figure 11: CMOS Inverter icon and layout with respective simulation SPICE scripts

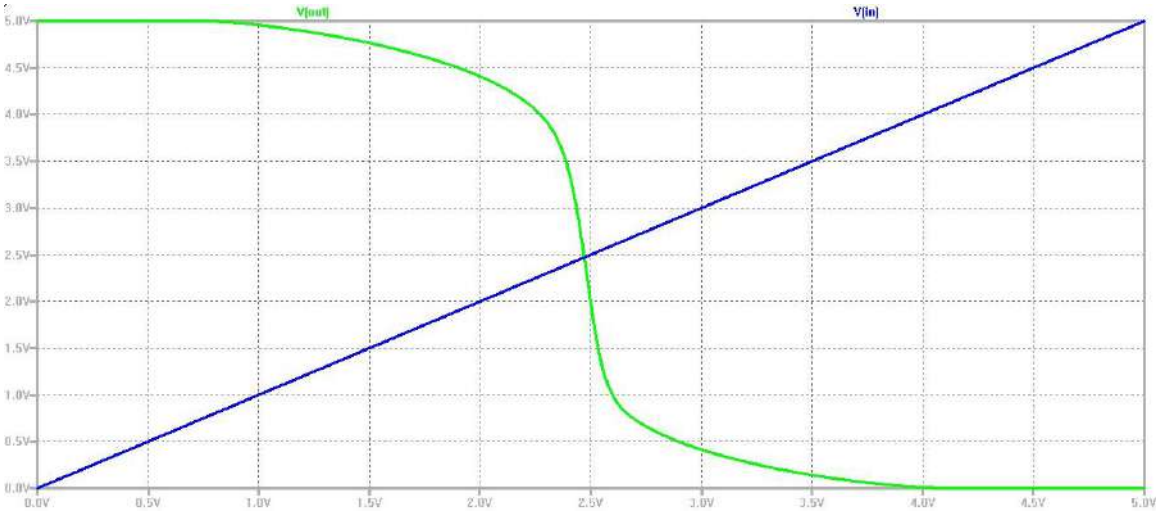


Figure 12: DC Characterstics for a CMOS Inverter

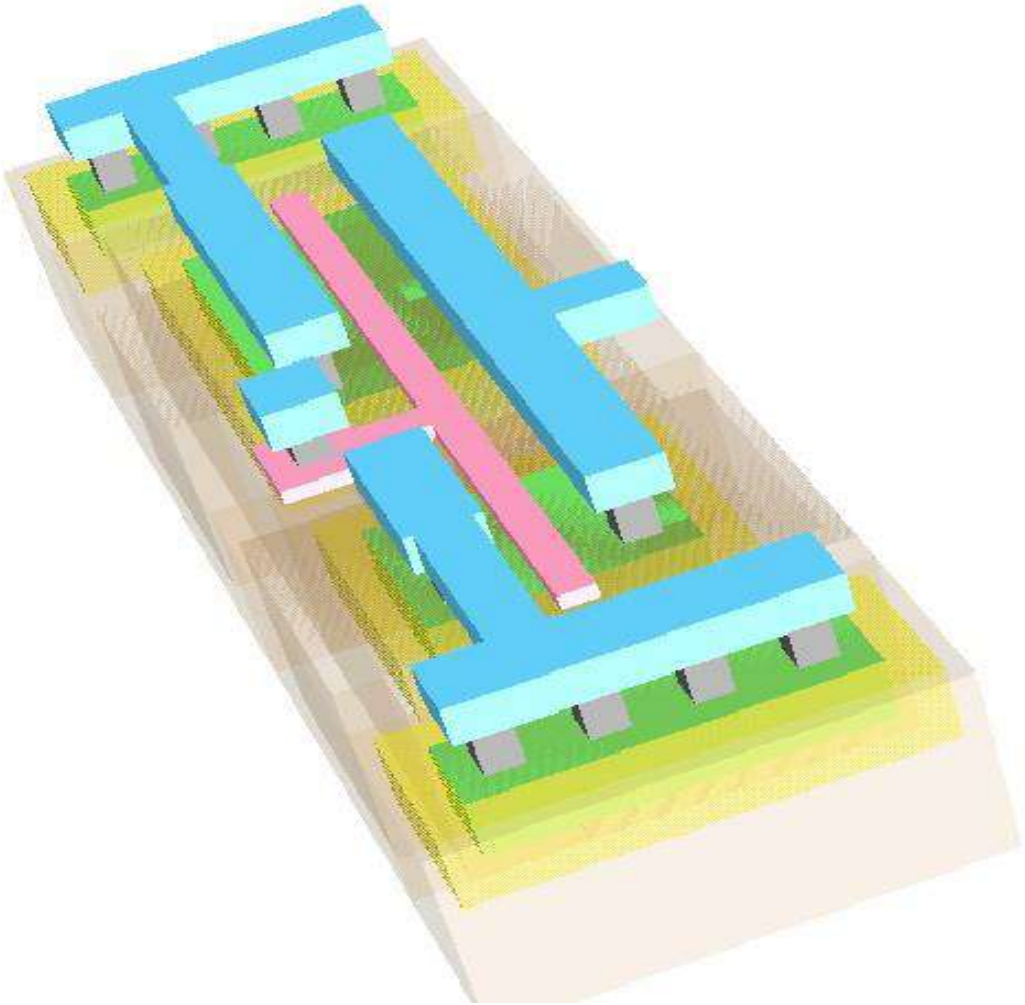


Figure 13: 3D View of a CMOS Inverter

Conclusion / Summary :

Design of Schematic and Layout and simulation and plotting of transient curves of CMOS Inverter was done. Design was done using C5 process technology.

Viva Questions

1. What is a substrate or Unprocessed wafer ?
2. What is patterning ? how N-well and P-well are patterned ?
3. What are active and poly layers in layout design ?
4. What is standard cell frame ?
5. How is n+ different from n and P+ different from p ?
6. What are various design rules for NMOS and PMOS layout design ?
7. What is ESD (Electrostatic Discharge Protection)?
8. What is a Spice Model ?
9. Write the spice script used for PMOS IV Simulation ?
10. Write the spice script used for NMOS IV Simulation ?

Experiment -6

Study of models for Analog IC Design and Digital IC Design and design of CMOS Cells.

Aim/Objective :

Study of models for Analog IC Design and Digital IC Design and design of CMOS Cells.

Theory :

The models presented for Analog and Digital IC Design are used for developing design equations, hand analysis and initial computer simulations. Both DC models, which are useful for biasing and large signal analysis and ac models which are useful for small signal sinusoidal steady state analysis.

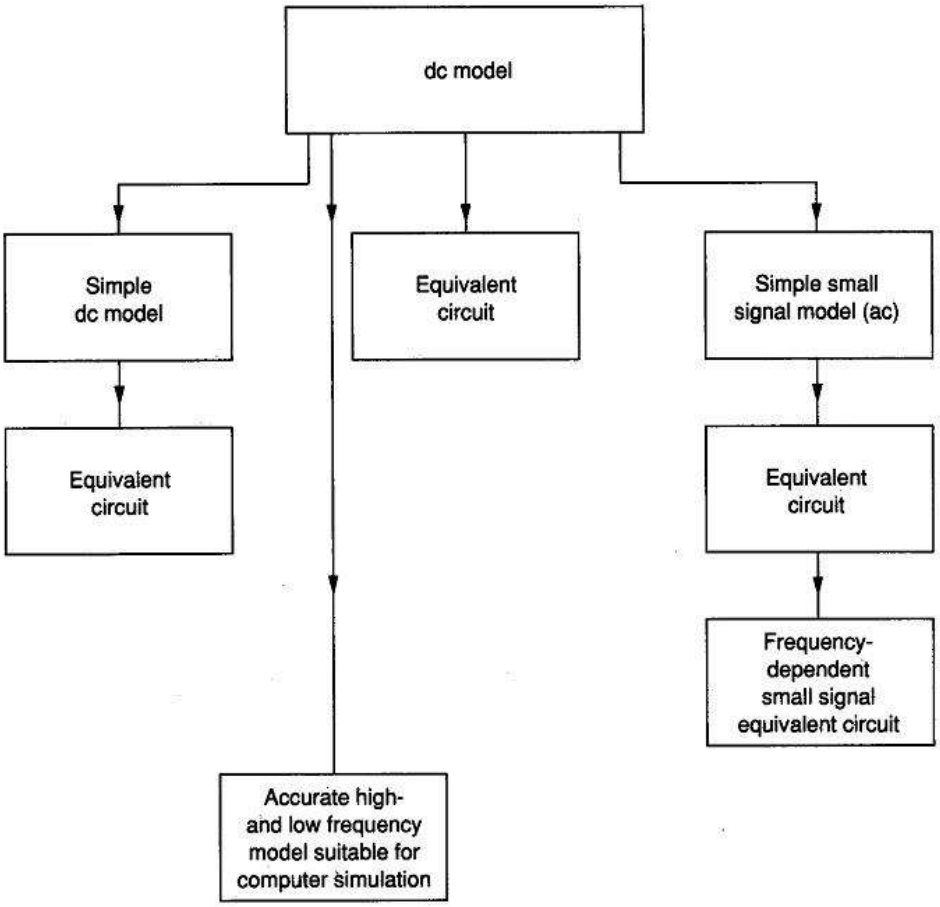


Figure 1: Approach to device modeling

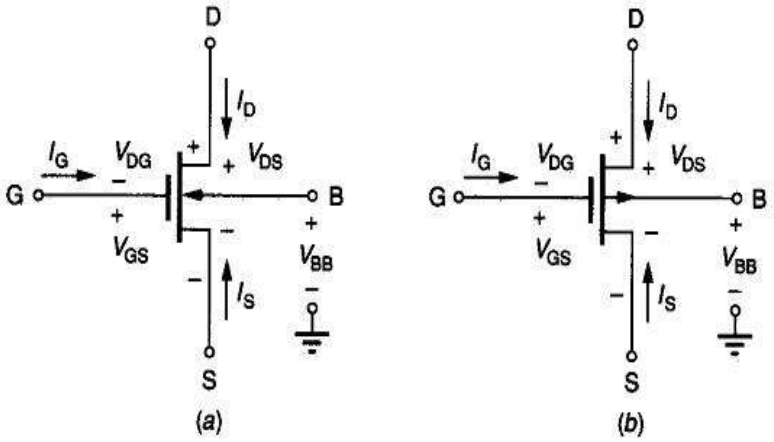


Figure 2: Basic voltage and current notations for MOSFET

Table 1
Low Frequency MOSFET Model

n-channel MOSFET

$$I_G = 0 \tag{1}$$

$$I_D = \begin{cases} 0 & V_{GS} < V_T \text{ (cutoff)}, \ V_{DS} \geq 0 \quad (2) \\ \dfrac{K'W}{L}\left(V_{GS} - V_T - \dfrac{V_{DS}}{2}\right) V_{DS} & V_{GS} > V_T, \ 0 < V_{DS} < V_{GS} - V_T \text{ (ohmic)} \quad (3) \\ \dfrac{K'W}{2L}(V_{GS} - V_T)^2 (1 + \lambda V_{DS}) & V_{GS} > V_T, \ V_{DS} > V_{GS} - V_T \text{ (saturation)} \quad (4) \end{cases}$$

where $$V_T = V_{T0} + \gamma(\sqrt{\phi - V_{BS}} - \sqrt{\phi}) \tag{5}$$

p-channel MOSFET

$$I_G = 0 \tag{6}$$

$$I_D = \begin{cases} 0 & V_{GS} > V_T \text{ (cutoff)}, \ V_{DS} \leq 0 \quad (7) \\ -\dfrac{K'W}{L}\left(V_{GS} - V_T - \dfrac{V_{DS}}{2}\right) V_{DS} & V_{GS} < V_T, \ 0 > V_{DS} > V_{GS} - V_T \text{ (ohmic)} \quad (8) \\ -\dfrac{K'W}{2L}(V_{GS} - V_T)^2 (1 - \lambda V_{DS}) & V_{GS} < V_T, \ V_{DS} < V_{GS} - V_T \text{ (saturation)} \quad (9) \end{cases}$$

where $$V_T = V_{T0} - \gamma(\sqrt{\phi + V_{BS}} - \sqrt{\phi}) \tag{10}$$

Design parameters:
- W = channel width
- L = channel length

Process parameters:
- K' = transconductance parameter
- V_{T0} = threshold voltage for $V_{BS} = 0$
- γ = bulk threshold parameter
- ϕ = strong inversion surface potential
- λ = channel length modulation parameter

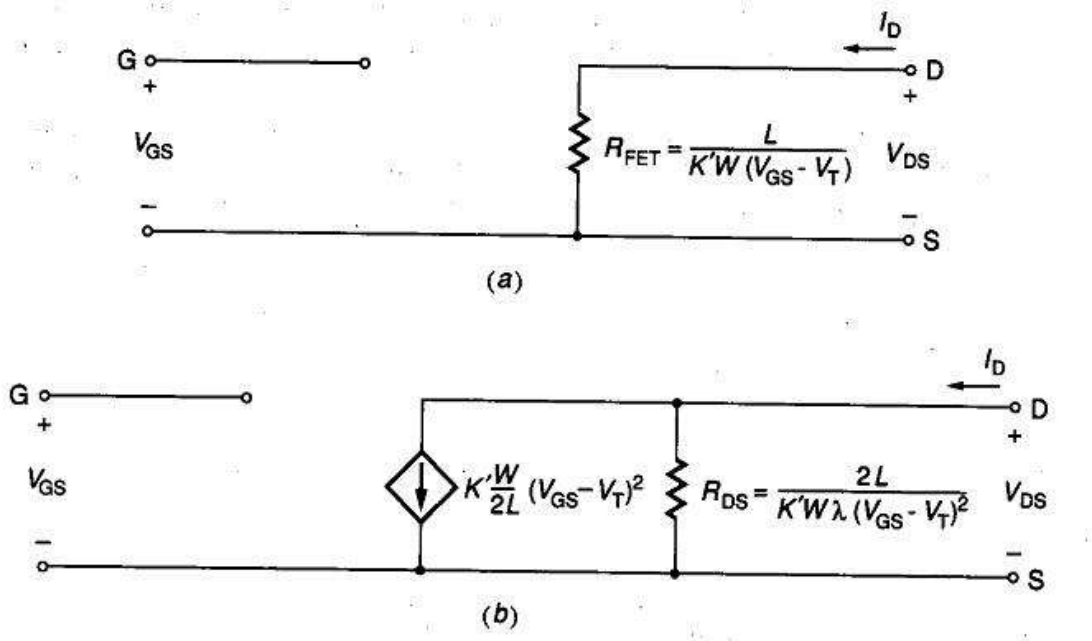


Figure 3 Equivalent Circuits of MOSFET in Ohmic Region and Saturation regions respectively

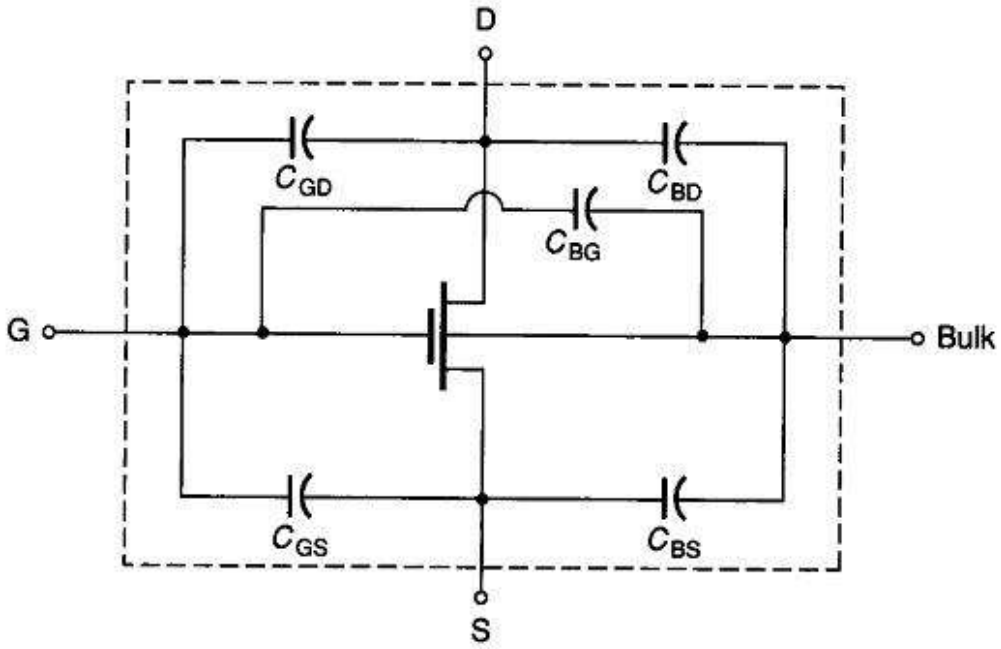
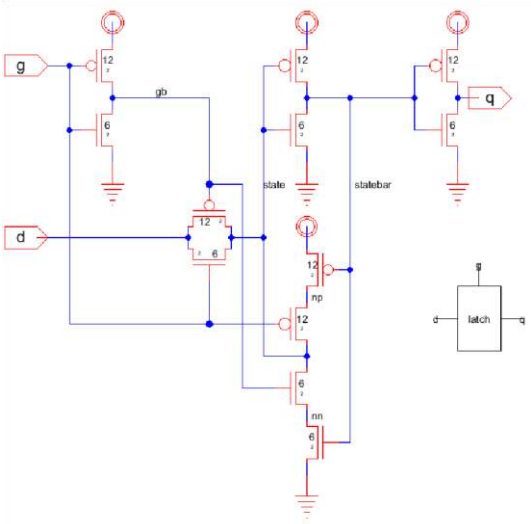
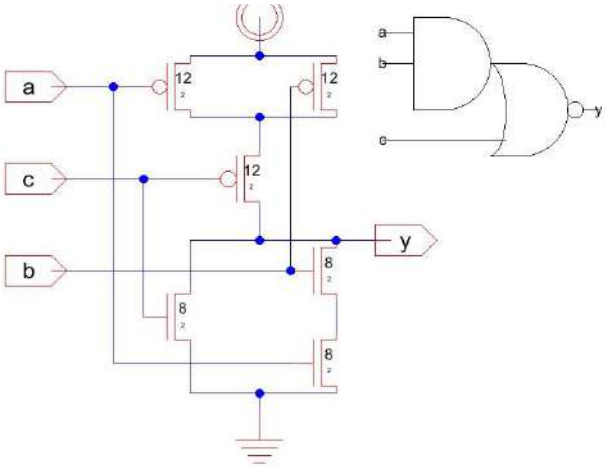
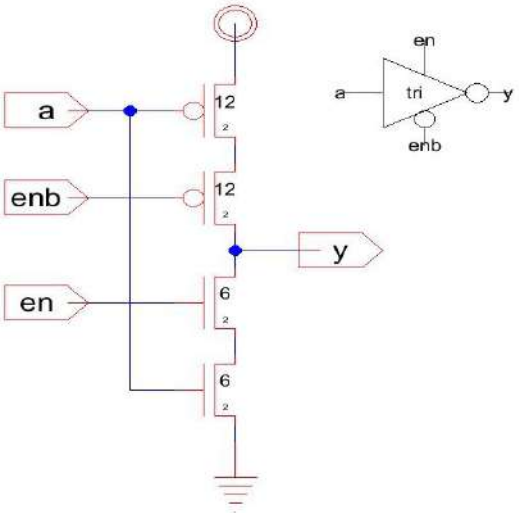


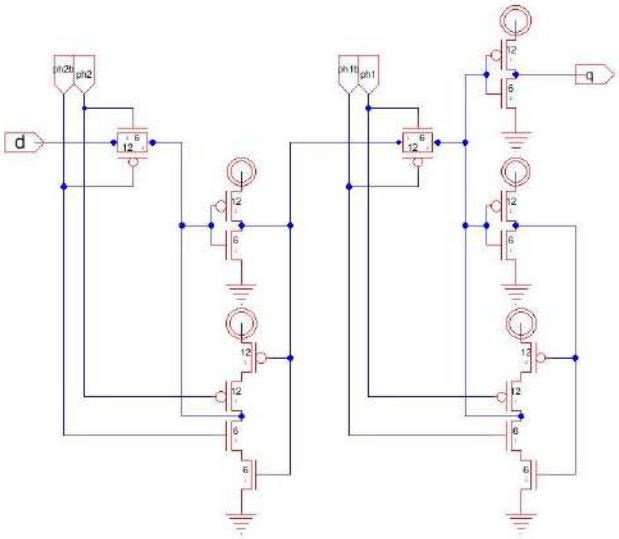
Figure 4: Capacitor lumped model

Few Standard Cells (Latches, Flops, Tristate Inv, AOI)









Conclusion / Summary :

Design of Schematic CMOS Standard cells was done. Design was done using C5 process technology. Additional DRC check was done on all the cells

Viva Questions

1. What is a substrate or Unprocessed wafer ?
2. What is patterning ? how N-well and P-well are patterned ?
3. What are active and poly layers in layout design ?
4. What is standard cell frame ?
5. How is n+ different from n and P+ different from p ?
6. What are various design rules for NMOS and PMOS layout design ?
7. What is ESD (Electrostatic Discharge Protection)?
8. What is a Spice Model ?
9. Write the spice script used for PMOS IV Simulation ?
10. Write the spice script used for NMOS IV Simulation ?

Experiment - 7

Design schematic, layout and simulation of CMOS NAND and NOR Gates.

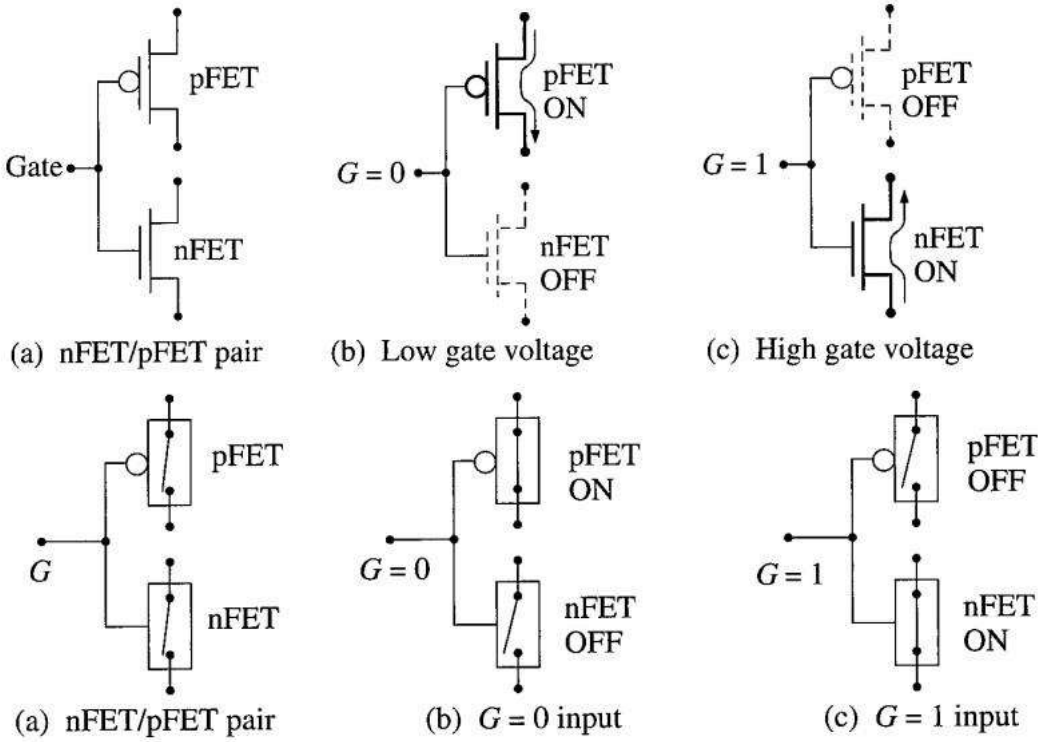
Aim/Objective:

Design schematic, layout and simulation of CMOS NAND and NOR Gates.

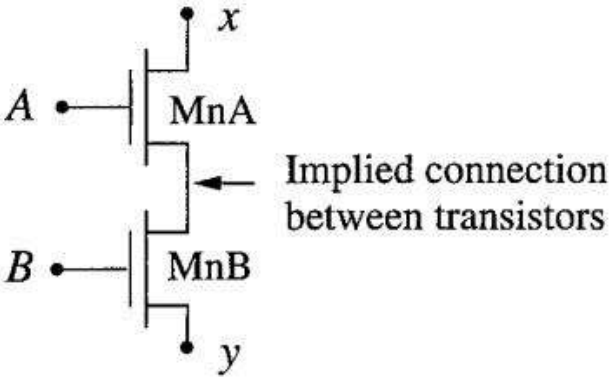
Theory :

Complementary pair of FETS

In digital electronics, a NAND gate (Negated AND or NOT AND) is a logic gate which produces an output that is false only if all its inputs are true; thus its output is complement to that of the AND gate. A LOW (0) output results only if both the inputs to the gate are HIGH (1); if one or both inputs are LOW (0), a HIGH (1) output results. The NOR gate is a digital logic gate that implements logical NOR - it behaves according to the truth table to the right. A HIGH output (1) results if both the inputs to the gate are LOW (0); if one or both input is HIGH (1), a LOW output (0) results. NOR is the result of the negation of the OR operator.

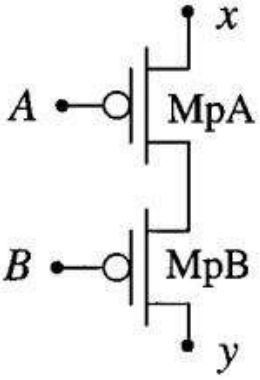


Series Connected MOSFETs



x is connected to y
if and only if
$A = 1$ AND $B = 1$

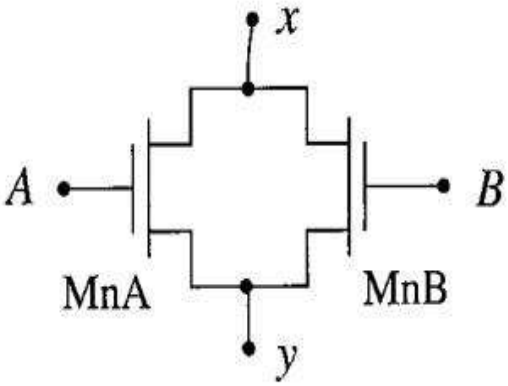
(a) nFET



x is connected to y
if and only if
$A = 0$ AND $B = 0$

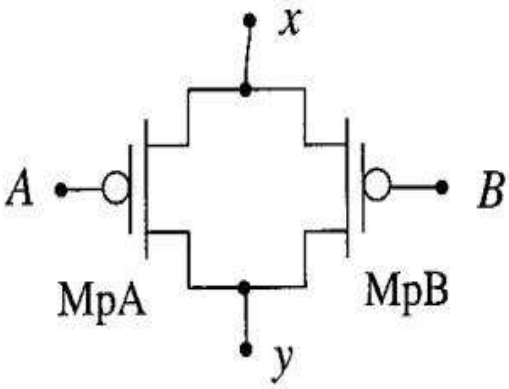
(b) pFET

Parallel Connected MOSFETs



x is connected to y
if either $A = 1$ OR
$B = 1$ (or both)

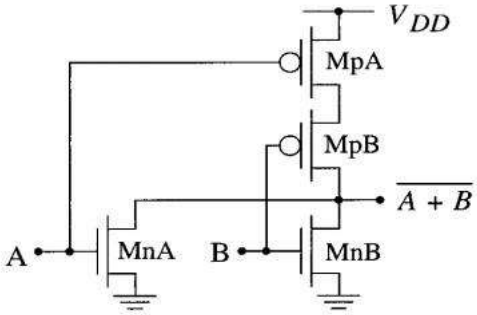
(a) nFETs



x is connected to y
if either $A = 0$ OR
$B = 0$ (or both)

(b) pFETs

CMOS NOR Gate

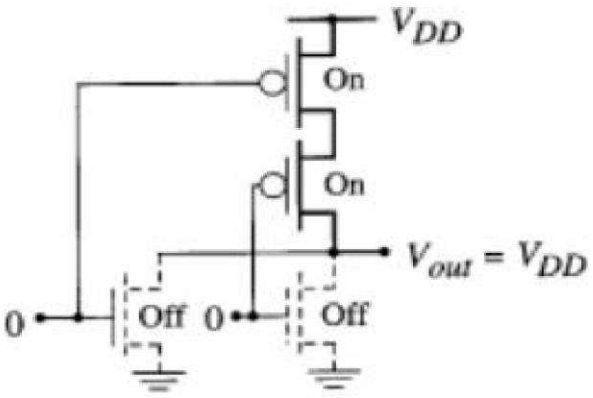


(a) CMOS circuit

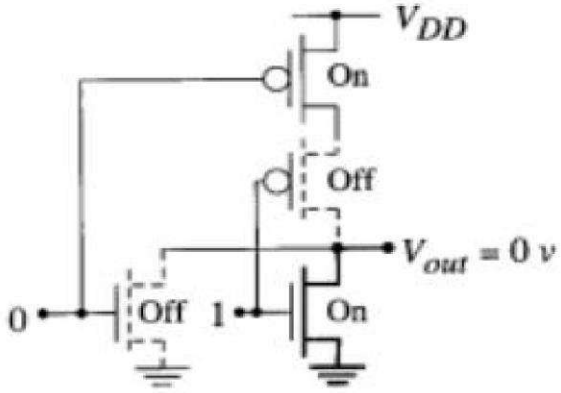
A	B	MnA	MnB	MpA	MpB	Out
0	0	OFF	OFF	**ON**	**ON**	1
0	**1**	OFF	**ON**	**ON**	OFF	**0**
1	0	**ON**	OFF	OFF	**ON**	**0**
1	**1**	**ON**	**ON**	OFF	OFF	**0**

(b) Operation summary

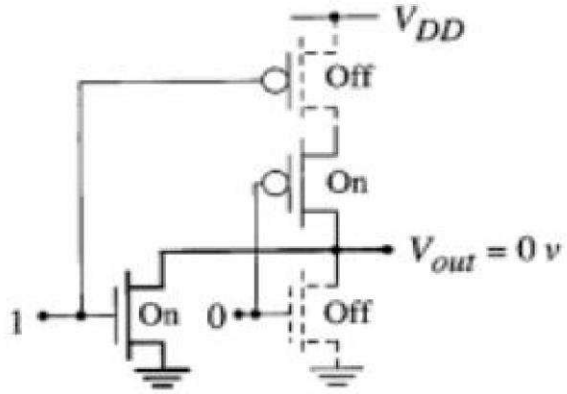
NOR gate Operation



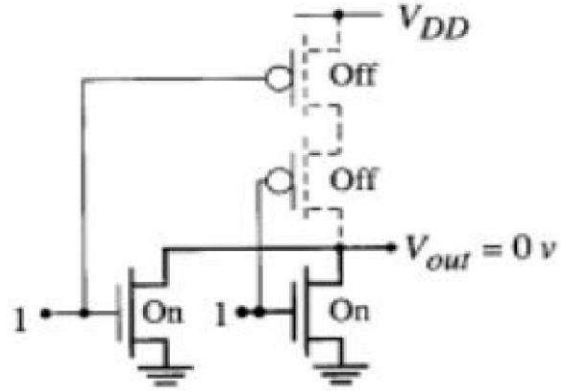
(a) $(AB) = (00)$



(b) $(AB) = (01)$

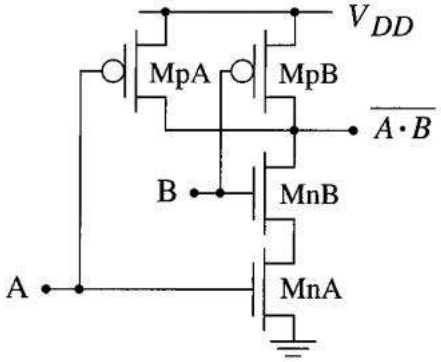


(c) $(AB) = (10)$



(d) $(AB) = (11)$

NAND Gate

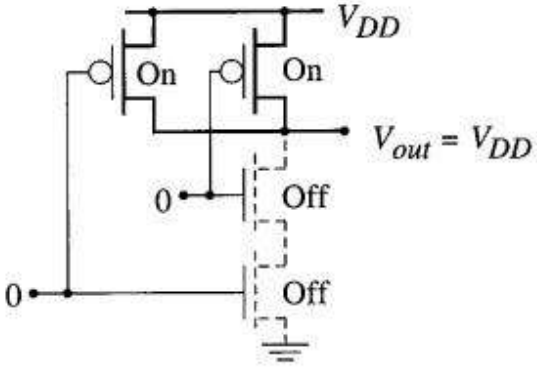


(a) CMOS circuit

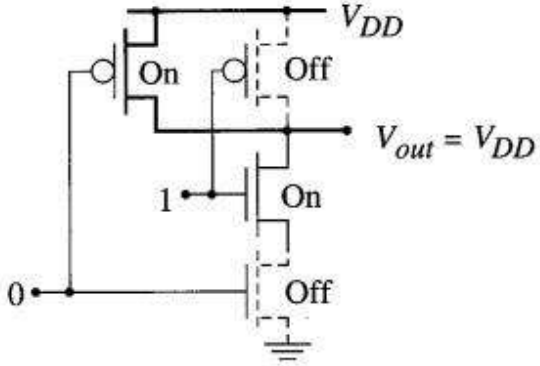
A	B	MnA	MnB	MpA	MpB	Out
0	0	OFF	OFF	**ON**	**ON**	1
0	1	OFF	**ON**	**ON**	OFF	1
1	0	**ON**	OFF	OFF	ON	1
1	**1**	**ON**	**ON**	OFF	OFF	**0**

(b) Operation summary

NAND Gate Operation



(a) $(AB) = (00)$



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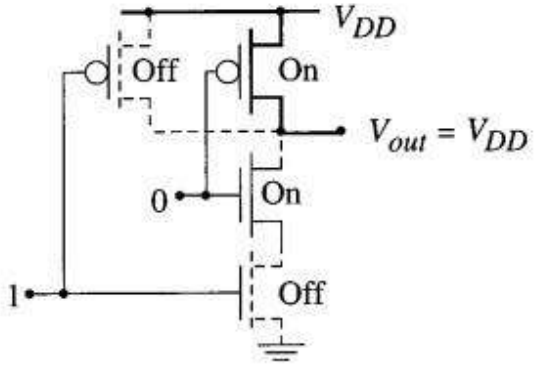
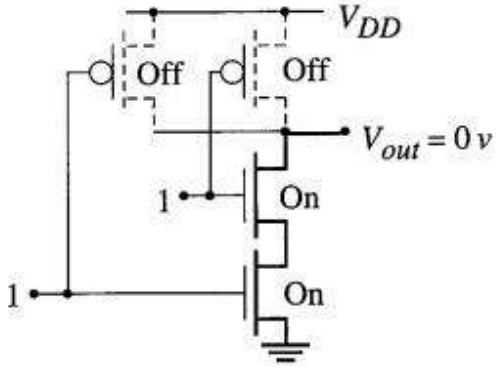
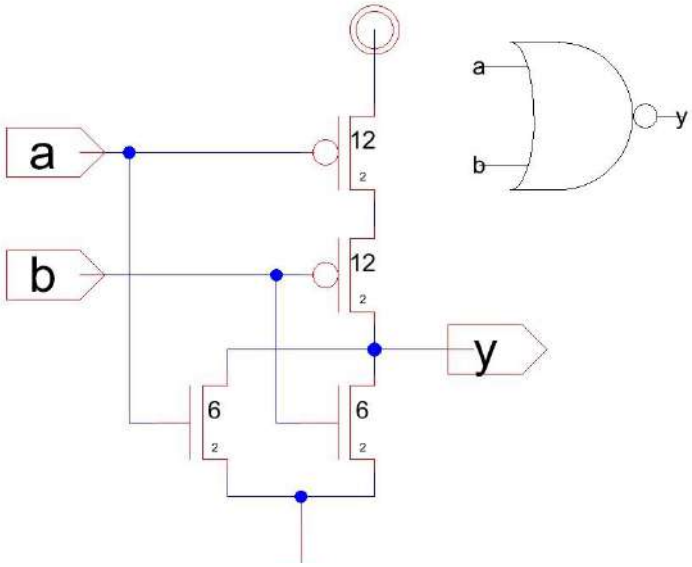


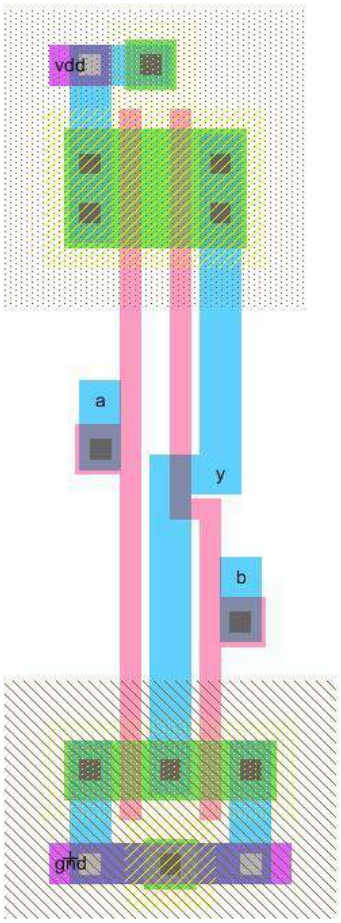
(c) $(AB) = (10)$

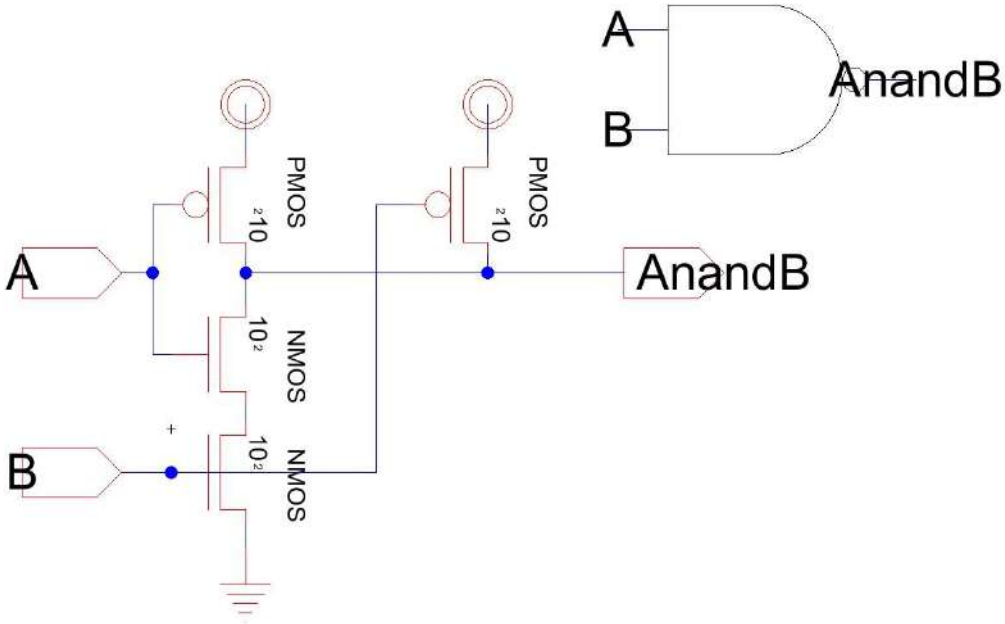


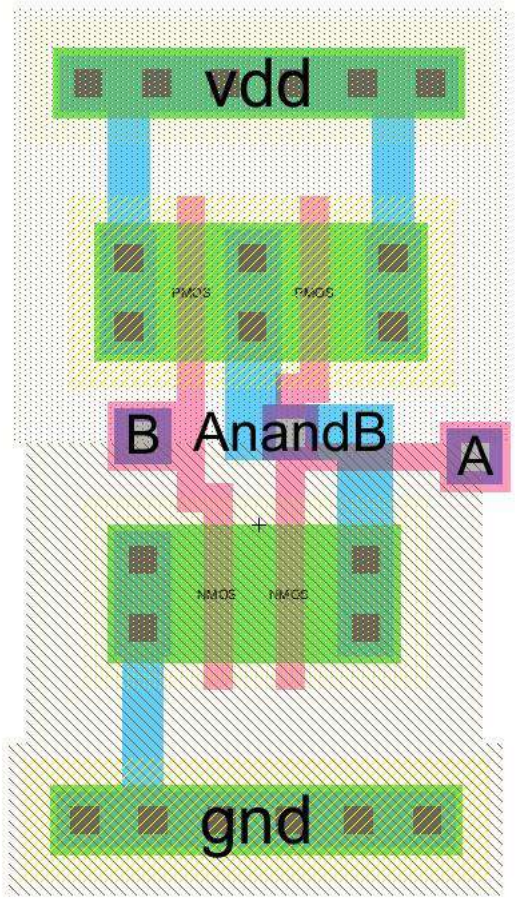
(d) $(AB) = (11)$

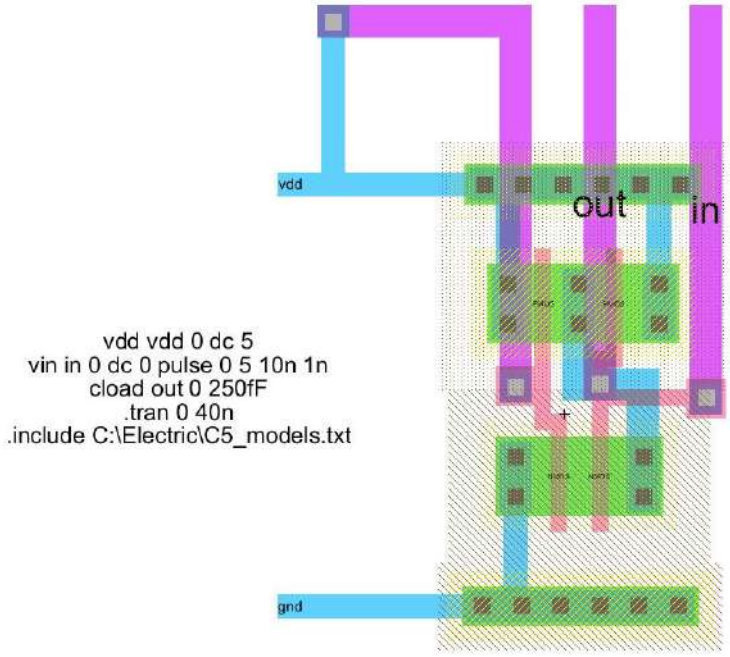
Simulation Results

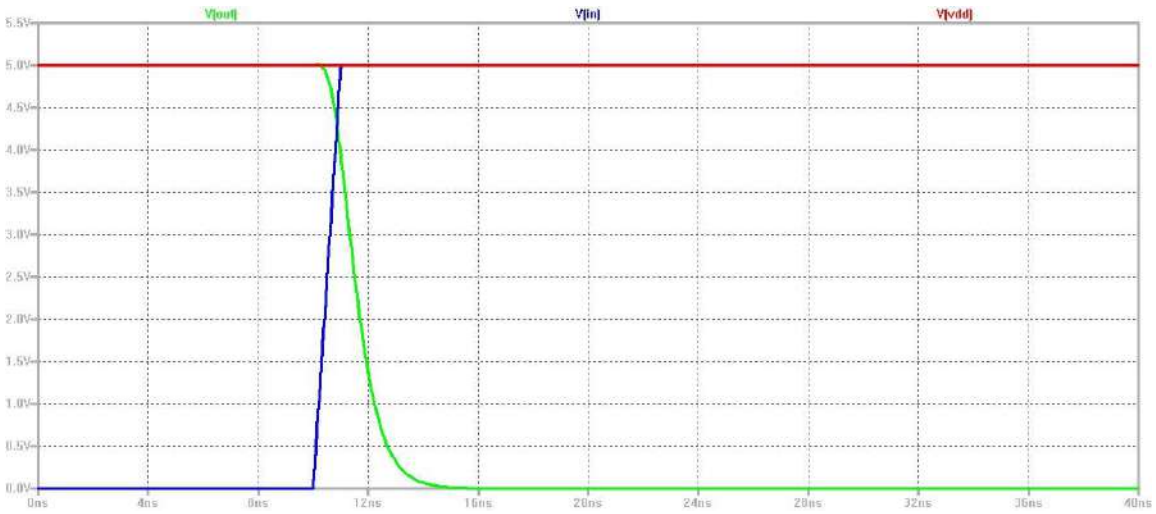

a
b
y
12
2
12
2
6
2
6
2


vdd
a
y
b
gnd


A
B
AnandB
PMOS
PMOS
NMOS
NMOS
A
B
AnandB


vdd
PMOS
PMOS
B
AnandB
A
NMOS
NMOS
gnd





Conclusion / Summary :

Designing of schematic, layout and simulation of CMOS NAND and NOR Gates was done and Design process is carried using C5 process technology .

Viva Questions

1. What is a substrate or Unprocessed wafer ?
2. What is patterning ? how N-well and P-well are patterned ?
3. What are active and poly layers in layout design ?
4. What is standard cell frame ?
5. How is n+ different from n and P+ different from p ?
6. What are various design rules for NMOS and PMOS layout design ?
7. What is ESD (Electrostatic Discharge Protection)?
8. What is a Spice Model ?
9. Write the spice script used for PMOS IV Simulation ?
10. Write the spice script used for NMOS IV Simulation ?

Experiment - 8

Design schematic, layout and simulation of Ring Oscillator

Aim/Objective:

Design schematic, layout and simulation of Ring Oscillator for

(a) 11 Stages

(b) 21 Stages

(c) 31 Stages

(d) 41 Stages

(e) 51 Stages **Theory :**

Voltage controlled Oscillators or Ring Oscillators are crucial components in any timing and memory circuits. The goal of this lab is to do physical design for a high speed, low power consumption multistage high performance ring oscillator circuit based on 300 nm CMOS technology which provides frequency of high order (KHz). This oscillator is used for high speed wireless communication applications and in control circuitries of numerous analog and digital integrated circuits. This ring oscillator is designed to be controlled in a oscillation frequency by a voltage input. The physical design will include C5 process, simultaneously various design rule check and network consistency checks were performed to improve performance characteristics of the oscillator. The Complementary-Metal-Oxide-Semiconductor (CMOS) is the most popular technology for the modern integrated circuit design and fabrication. Based on this technology, a VCO can be implemented by the LC resonant or Ring structure. In this paper a ring based VCO is design which has small chip area, low power consumption which is suitable for wide tuning band VCO of namely 11 stages, 21 stages and 51 stages. The paper will also focus on various design considerations namely basic cell design, bias circuitry and design implementation and testing of the same.

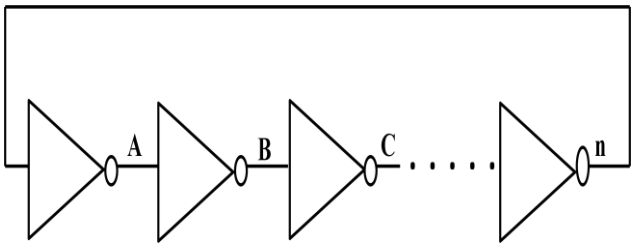


Fig.1 Ring Oscillator realization with n digital inverters

DESIGN AND SIMULATION RESULTS

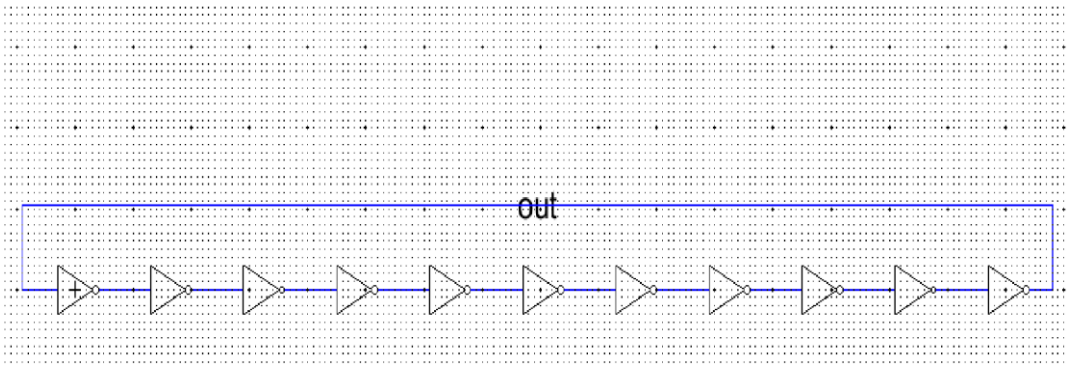


Fig.2 Schematic of 11 stage Ring Oscillator

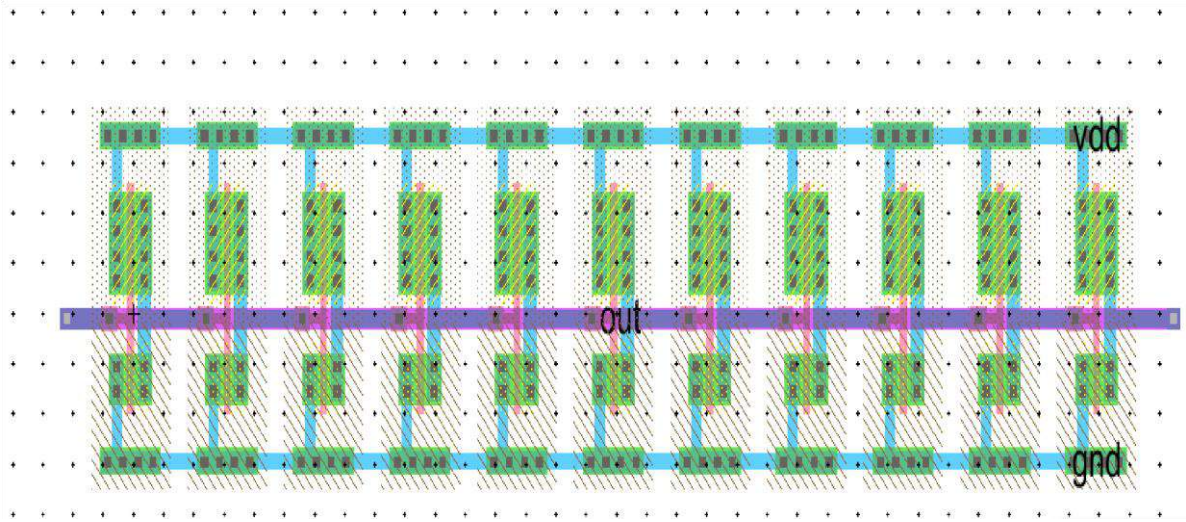


Fig.3 Layout of 11 stage Ring Oscillator

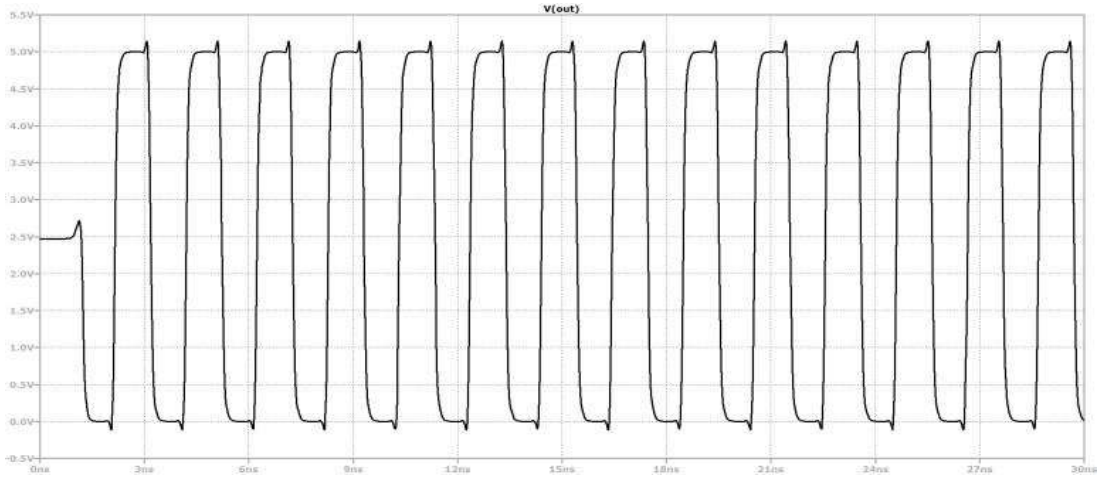


Fig.4 Transient plot for 11 stage Ring Oscillator

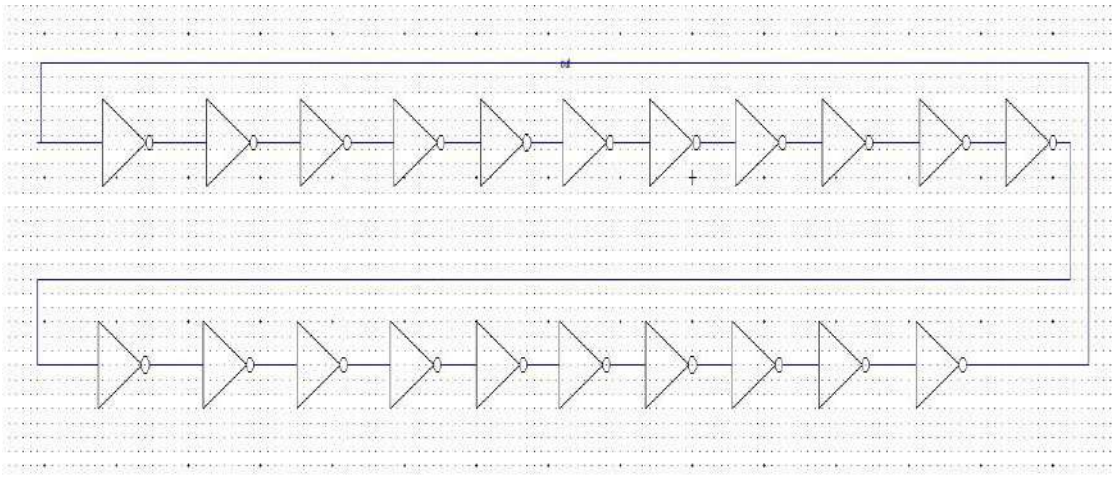


Fig.5 Schematic of 21 stage Ring Oscillator

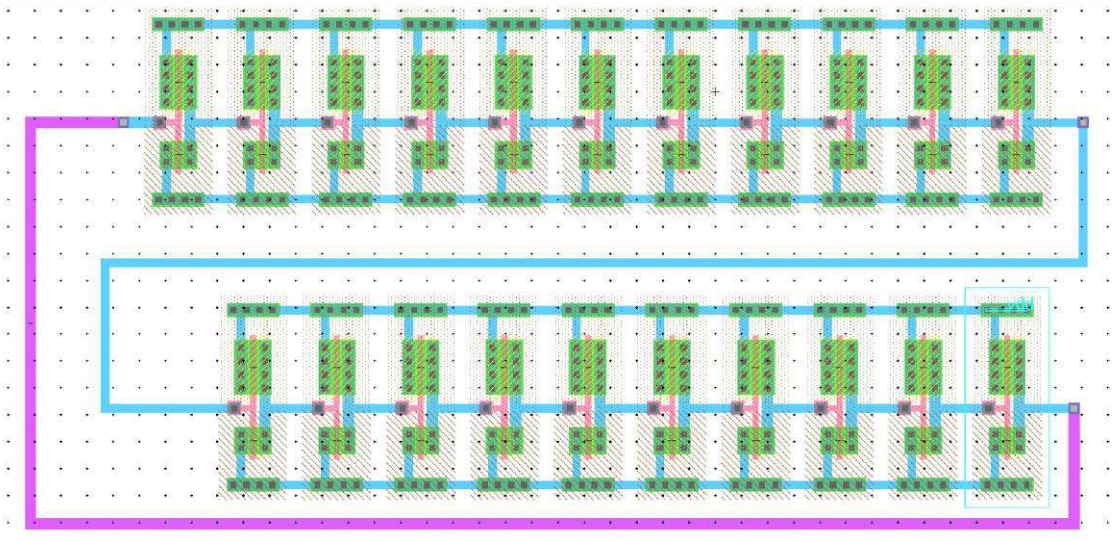


Fig.6 Layout of 21 stage Ring Oscillator

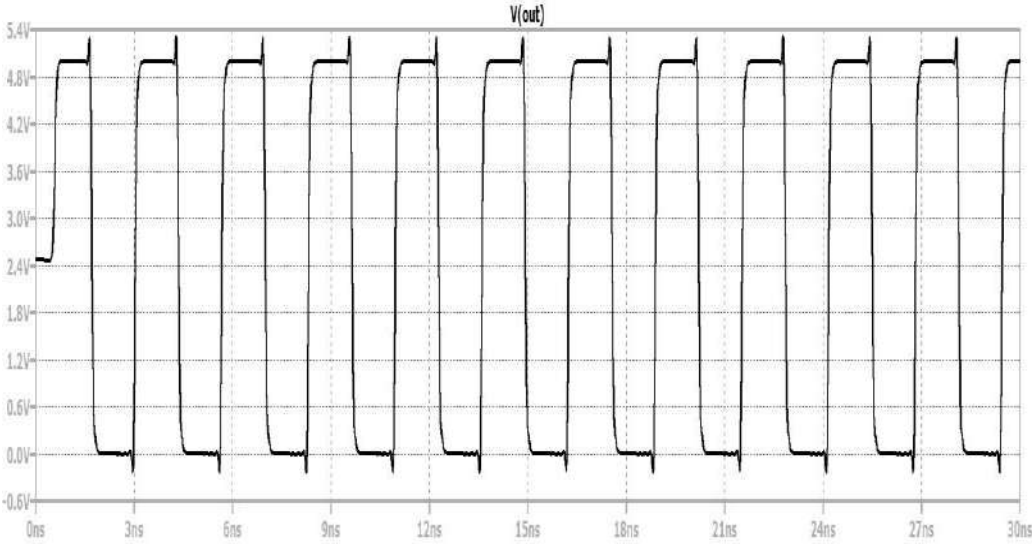


Fig.7 Simulation plot for 21 stage Ring Oscillator

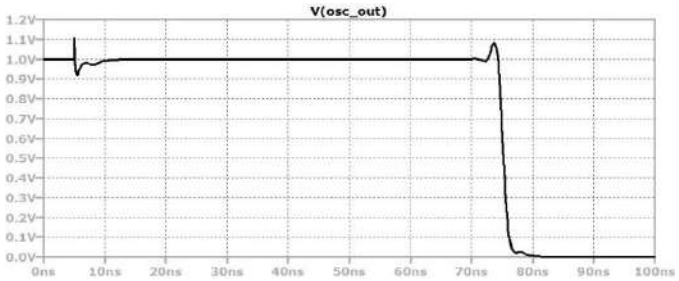


Fig.8 Simulation plot for 51 stage Ring Oscillator (Transient 30 n)

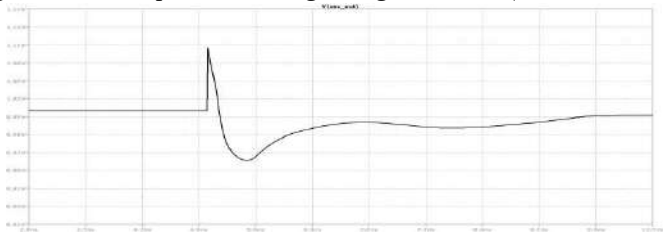


Fig.9 Simulation plot for 51 stage Ring Oscillator (Transient 100n)

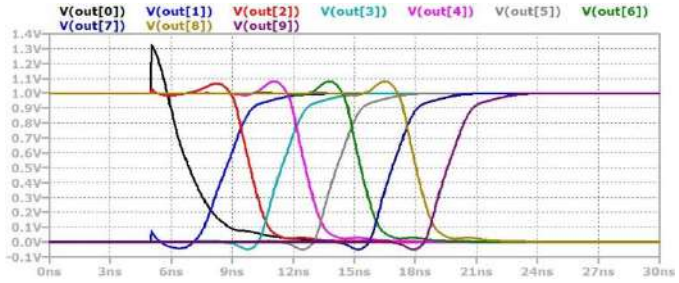


Fig.10 Simulation plot for 51 stage Ring Oscillator
(Output of first 10 stages)

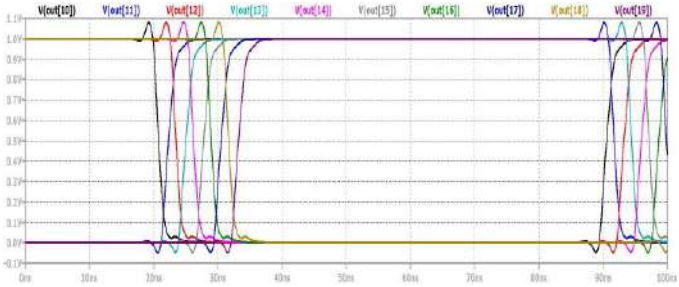


Fig.11 Simulation plot for 51 stage Ring Oscillator
(Output of 10-20th stages)

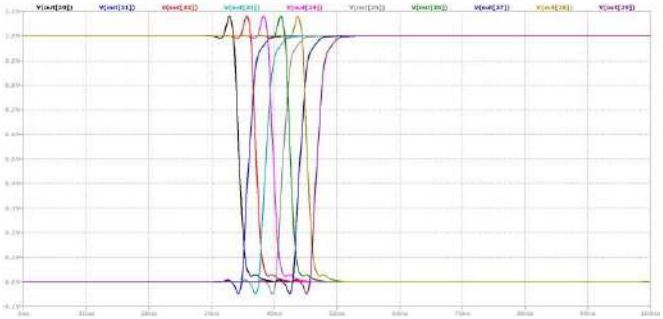


Fig.12 Simulation plot for 51 stage Ring Oscillator
(Output of 20-30thstages)

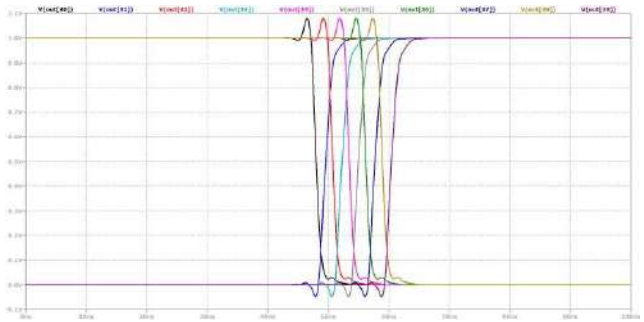


Fig.13 Simulation plot for 51 stage Ring Oscillator
(Output of 30-40th stages)

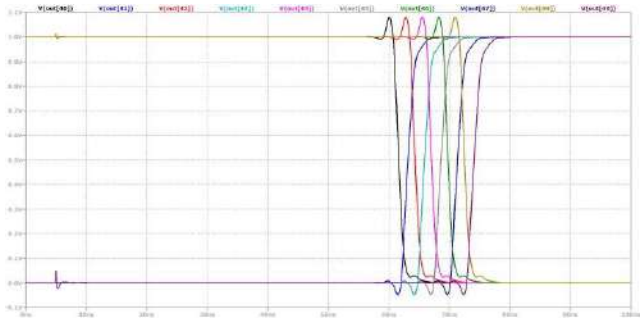


Fig.14 Simulation plot for 51 stage Ring Oscillator
(Output of 40-50thstages)

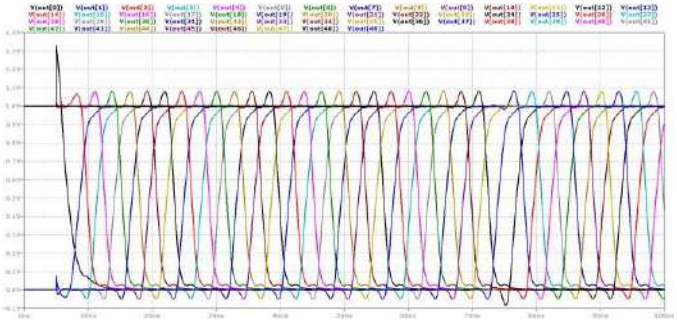


Fig.15 Simulation plot for 51 stage Ring Oscillator (Output of individual 51 stages)

Conclusion / Summary :

Designing of schematic, layout and simulation of Ring Oscillator was done and Design process is carried using C5 process technology.

Viva Questions

1. What is a substrate or Unprocessed wafer ?
2. What is patterning ? how N-well and P-well are patterned ?
3. What are active and poly layers in layout design ?
4. What is standard cell frame ?
5. How is n+ different from n and P+ different from p ?
6. What are various design rules for NMOS and PMOS layout design ?
7. What is ESD (Electrostatic Discharge Protection)?
8. What is a Spice Model ?
9. Write the spice script used for PMOS IV Simulation ?
10. Write the spice script used for NMOS IV Simulation ?

Experiment - 9

Design and Simulation of Operational Amplifier

Aim/Objective:

Design and simulation of Operational Amplifier

(a) Two Stage

(b) Three Stage

(c) Perform AC, DC, and transient analysis for each of the above configurations of Operational Amplifier

Theory:

Operational amplifiers with low voltage supply requirements, low static power dissipation, rail to rail output swing and high slew rate are desirable in applications where power dissipation efficiency is critical such as portable electronics i.e. amplifiers, active filters, arithmetic circuits, logarithmic and antilogarithmic amplifiers, comparator circuits, waveform generators, precision rectifiers, multipliers, timers and regulated power supplies. Developing circuit architectures for these characteristics and implementing them in portable electronics applications will let the consumers enjoy the product longer before recharging and replacing their batteries. An operational amplifier is a fundamental building block in analog integrated circuit design and is used to realize functions ranging from DC bias generation to high speed amplification or filtering. There are numerous number of configurations for Operational amplifiers exist in literature. The classification of the namely existing topologies includes single stage, two stage, three stage and multistage amplifiers. By reasons that will become evident later on in this report two stage and three stage topologies are the best choice for the low voltage and high performance applications.

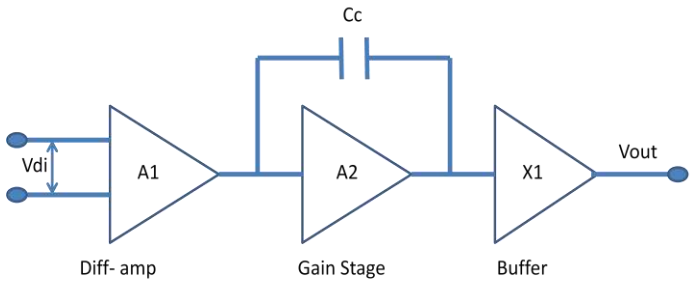


Fig 1.1 Block Diagram of 2 stage Operational Amplifier with output buffer.

Op-amp performance parameters

As a designer, the knowledge of Op-amp parameters is of great help. The clear understanding and meaning has its impact on the design. The selection of any Op-amp must be based on the understanding of what particular parameters are most important to the application. The following is the list of various parameters

1. Large signal Voltage Amplification Av
2. Differential Voltage Amplification AVD

3. Unity Gain Bandwidth
4. Gain Bandwidth Product
5. Gain Margin
6. Phase Margin
7. Common Mode Rejection Ratio
8. Supply Voltage Rejection Ratio
9. Slew Rate
10. Common mode input voltage range
11. Equivalent input noise voltage
12. Input resistance
13. Differential input resistance
14. Output resistance
15. Input offset voltage, Vio
16. Input offset current Iio
17. Input bias current

1.Large signal Voltage Amplification (Av)

The open loop of an Op-amp determines the precision of the feedback system employing the Op-amp. The required gain can be adjusted according to the application. Trading with the parameters such as speed and output voltage swings, the minimum required gain must therefore be known. A high open loop gain is also necessary to suppress nonlinearity. Av is the ratio of the peak to peak output voltage swing to the change in the input voltage required to drive the output.

$$Av = \frac{Vo(p-p)}{Vin}$$

2.Differential Voltage Amplification (AVD)

The ratio of the change in the output to the change in the differential input voltage producing it with the common mode input voltage held constant.

$$Avd = \Delta \frac{Vo}{\Delta Vin} \mid \text{Vincmcnst.}$$

3.**Unity Gain Bandwidth**

The range of frequencies with in which the open loop voltage amplification is greater than unity.

4.Gain Bandwidth Product

The product of the open loop voltage amplification and the frequency at which it is measured.

$$GBW = A1 * \omega 1$$

5.Gain Margin

The reciprocal of he open loop voltage amplification at the lowest frequency at which the open loop phase shift is such that the output is in phase with the inverting input.

6.Phase Margin

The absolute value of the open loop phase shift between the output and the inverting input on the frequency at which the modulus of the open loop amplification is unity. Gain and phase margins are measures of stability for a feedback system though often only phase margin is used rather than both. Based on the magnitude response of the loop gain |Av|, gain margin is the difference between unity and |Av (w180̊)| where W180̊ is the frequency at which the loop gain phase is 180̊ called as Phase crossover frequency. Phase margin is the difference between phase of Av (W0dB) and -180̊ where W0dB is the frequency at which |Av| is unity called unity gain frequency.

7.Common Mode Rejection Ratio

The ratio of differential voltage amplification to common mode voltage amplification. CMRR falls off as the frequency increases.

$$CMRR = ADIFF / ACOM$$

ACOM is measured by determining the ratio of a change in the input common mode voltage to the resulting change in the input offset voltage.

8.Supply Voltage Rejection Ratio

The absolute value of the ratio of the change in the supply voltages to the change in the input offset voltage.

$$SVRR = \Delta\frac{Vcc}{\Delta Vos}$$

9.Slew Rate

The average time rate of change of the closed loop amplifier output voltage for a step signal input.

$$SR = \frac{dv}{dt}$$

In Op-amps, we trade power consumption for noise and speed. To increase slew rate the bias currents within the Op-amps are increased.

10. Common mode input voltage range VICR

The range of common mode input voltage that if exceeded may cause the operational amplifier to cease functioning properly.

11. Equivalent input noise voltage Vn

The voltage of an ideal voltage source (having internal impedance equal to zero) in series with the input terminals of the device that represents the part of the internally generated noise that can be properly represented by a voltage source.

12.Input resistance (Ri)

The resistance between the input terminals with either input grounded.

13.Differential input resistance Rid

The small signal resistance between two ungrounded input terminals.

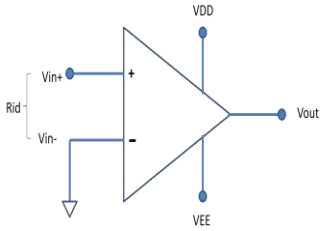


Fig. 2 Input Differential Resistance

14.Output resistance (Ro)

The resistance between output terminal and ground.

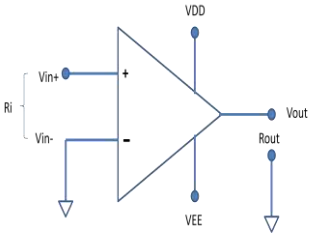


Fig. 3 Showing input and Output Resistance

15.Input offset voltage (Vio)

The dc voltage that must be applied between the input terminal to force the quiescent dc output voltage to zero or any other level, if specified.

16.Input offset current (Iio)

The difference between the currents into the two input terminals with the ouput at the specified level.

17.Input bias current (IB)

The average of the currents into the two input terminals with the output at the specified level.

$$I_B = \frac{I_{b+} + I_{b-}}{2}$$

$$I_{io} = I_{b+} + I_{b-}$$

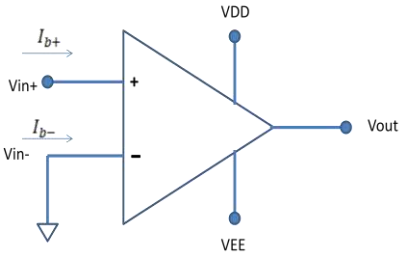


Fig.4 Op-amp input bias current and input offset current

Simulation Results

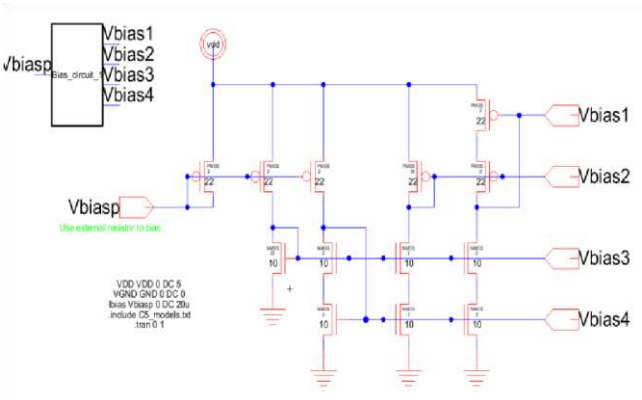


Fig. 5 Opamp Biasing Circuitry

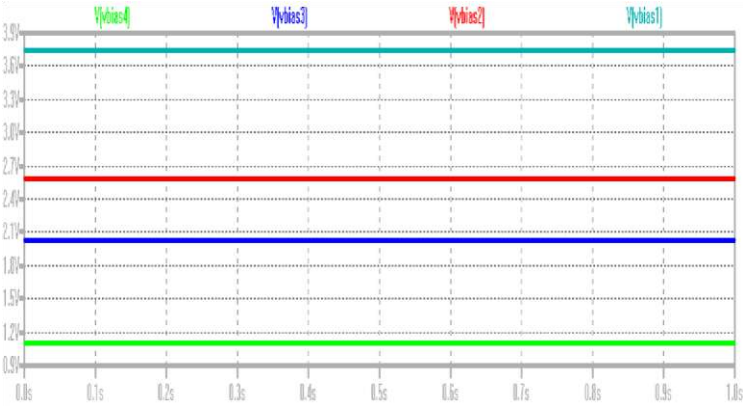


Fig. 6 Opamp Biasing Circuitry Simulation Results

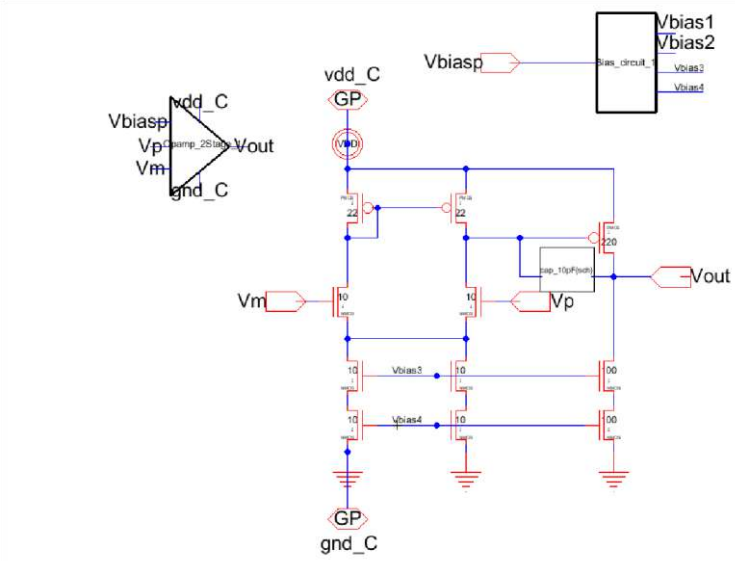


Fig. 7 Opamp 2 Stage Configuration

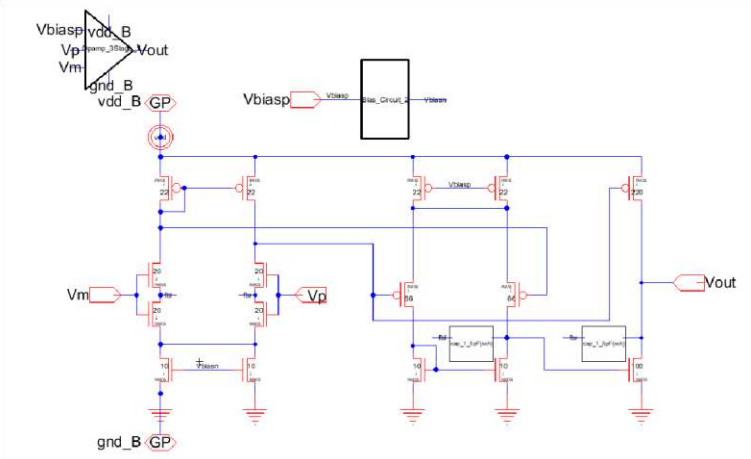


Fig.8 Opamp 3 stage Configuration

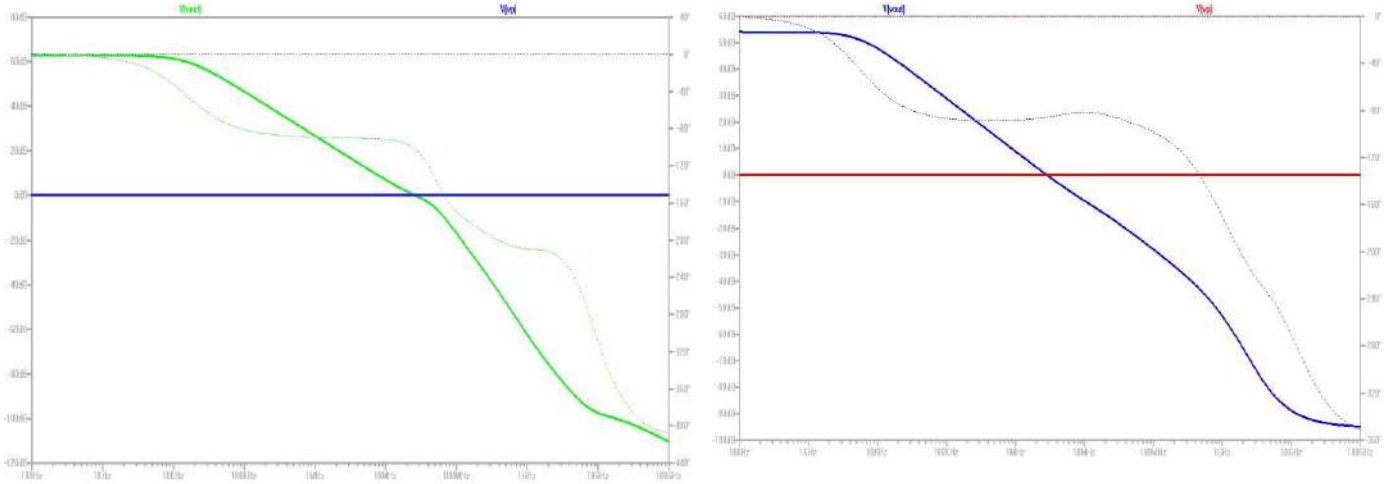


Fig. 9 AC analysis of 2 stage and 3 stage amplifiers

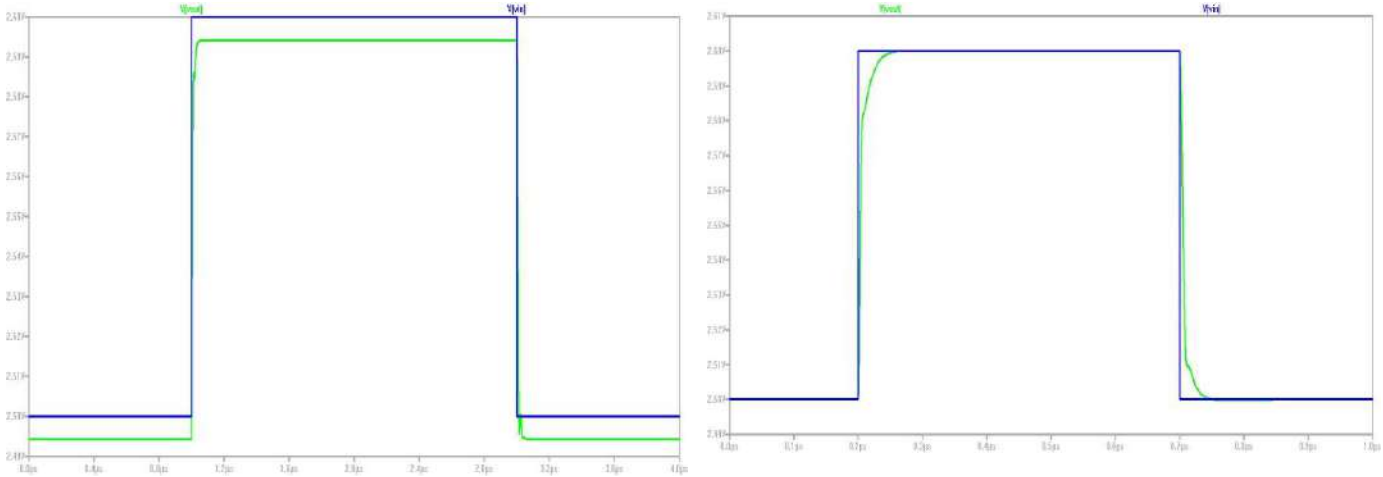


Fig.10 Transient analysis for 2 and 3 stage amplifiers

Results

Following are the parameters obtained

Parameters	Topology1	Topology2	Topology3	Topology4
Gain(dB)				
UGB_{3dB} (KHZ)				
UGB (MHZ)				
CMRR (dB)				
Phase margin (degree)				
Positive Slew Rate (v/µs)				
Negative slew rate (v/µs)				
Gain margin (dB)				
Rise time(ns)				
3% settling Time (ns)				
Output swing (at vdd 5volt)				

Conclusion / Summary :

Design and analysis of Operational Amplifier was done and Design process is carried using C5 process technology.

Lakshmi Narain College of Technology, Bhopal

Viva Questions

1. What is a substrate or Unprocessed wafer ?
2. What is patterning ? how N-well and P-well are patterned ?
3. What are active and poly layers in layout design ?
4. What is standard cell frame ?
5. How is n+ different from n and P+ different from p ?
6. What are various design rules for NMOS and PMOS layout design ?
7. What is ESD (Electrostatic Discharge Protection)?
8. What is a Spice Model ?
9. Write the spice script used for PMOS IV Simulation ?
10. Write the spice script used for NMOS IV Simulation ?

Experiment - 10

Design and Placing circuit layouts in a pad frame for fabrication

Aim/Objective:

Design and Placing circuit layouts in a pad frame for fabrication

Following are the circuits to be placed on padframe

(a) Inverter

(b) NAND Gate

(c) Ring Oscillator

Theory:

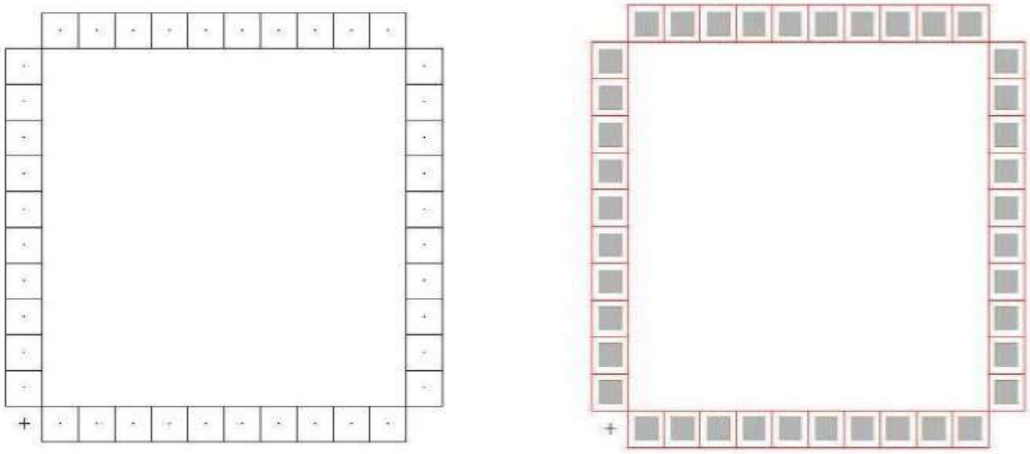


Fig. 1 Basic Padframes

The Pad Frame generator reads a disk file and places a ring of pads around your chip. The pads are contained in a separate library, and are copied into the current library to construct the pad frame. The format of the pad frame disk file is as follows:

1. celllibrary LIBRARYFILE	; Identifies the file with the pads
2. cell PADFRAMECELL	; Creates a cell to hold the pad frame
3. views VIEWS	; A list of views to generate
4. core CORECELL	; Places cell in center of pad frame
5. align PADCELL INPUTPORT OUTPUTPORT	; Defines input and output ports on pads
6. export PADCELL IOPORT [COREPORT]	; Defines exports on the pads
7. place PADCELL [GAP] [PORTASSOCIATION]	; Places a pad into the pad frame
8. rotate DIRECTION	; Turns the corner in pad placement

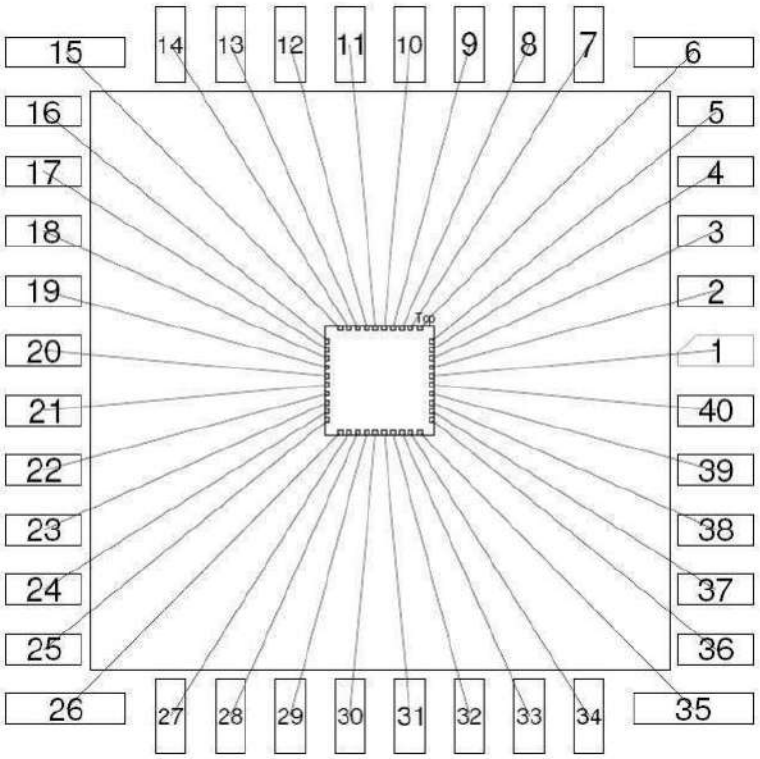


Fig. 2 Package Connectivity

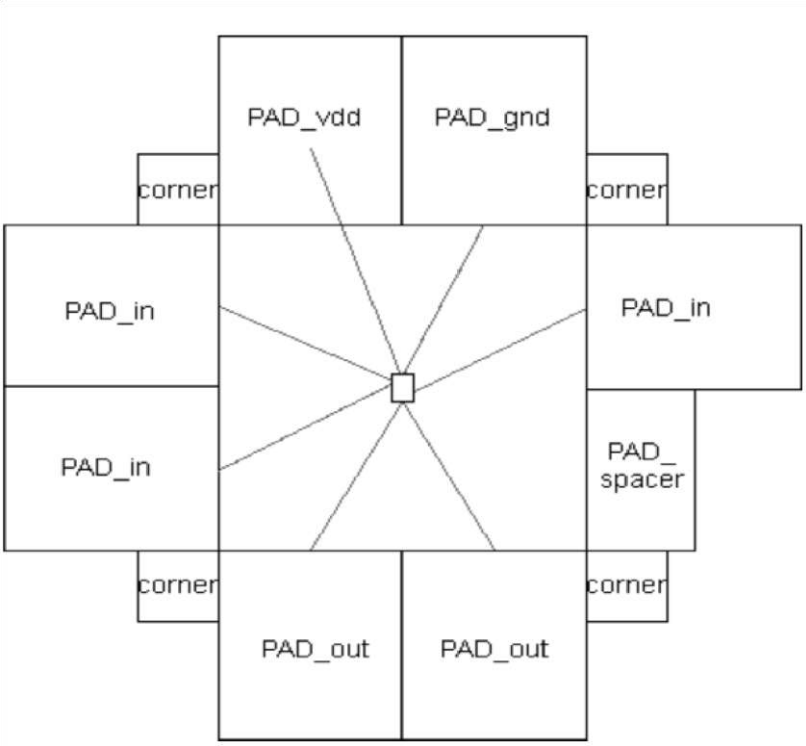


Fig. 3 Package Connectivity detailed

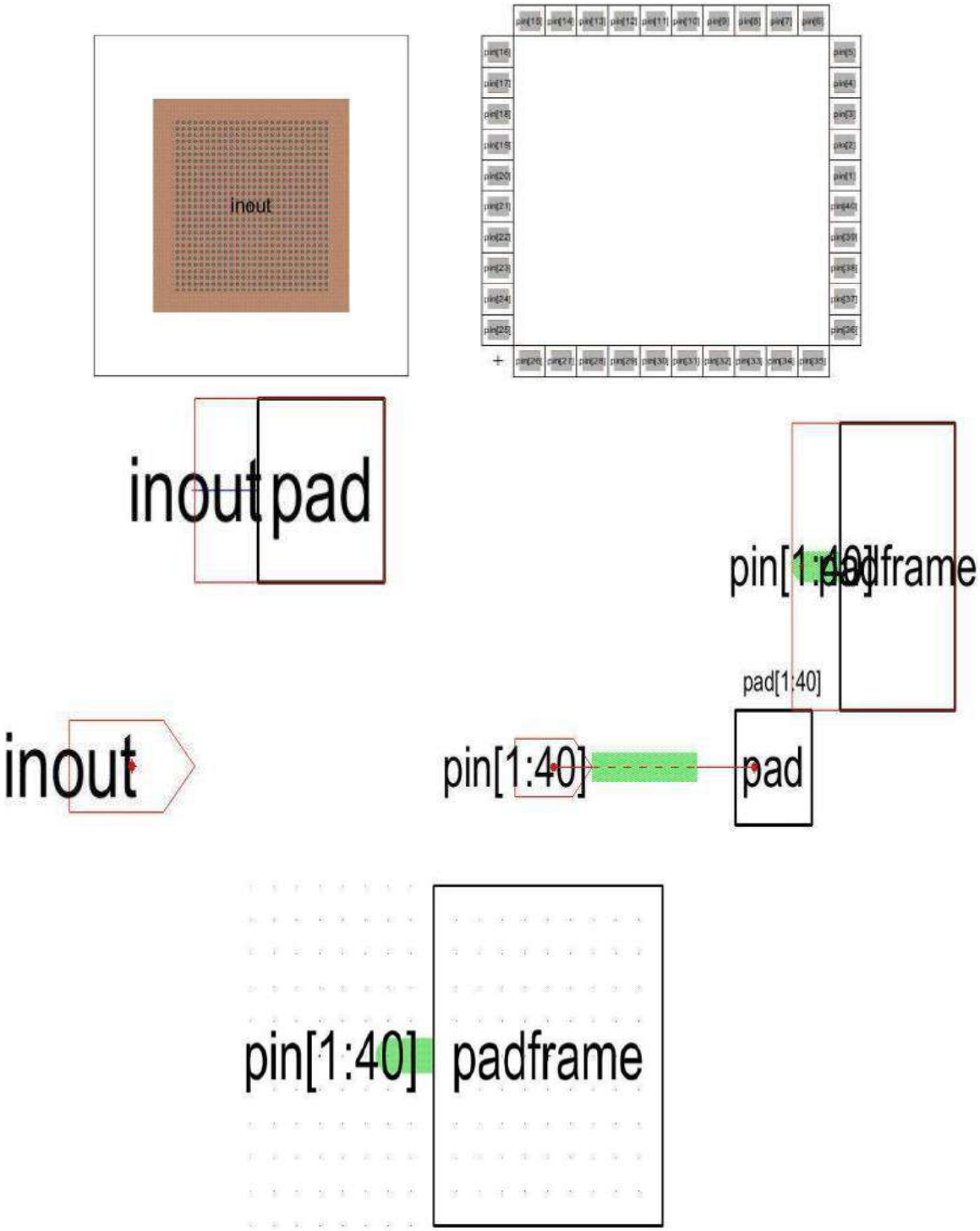
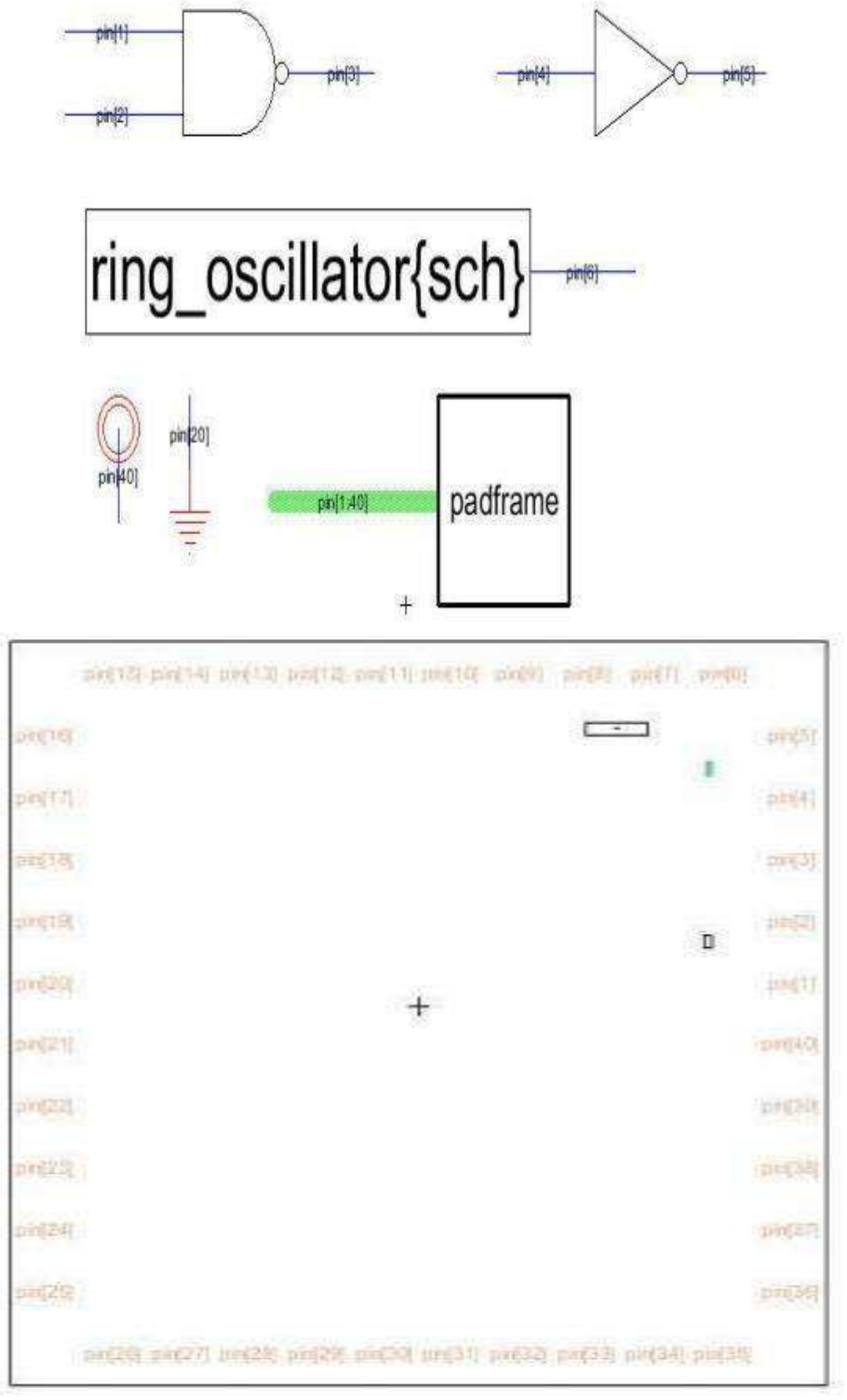

inout
inout
pad
pin[1:40]
padframe
pad[1:40]
inout
pin[1:40]
pad
pin[1:40]
padframe

Fig. 4 Fabricating Pad frame procedure

Result Chip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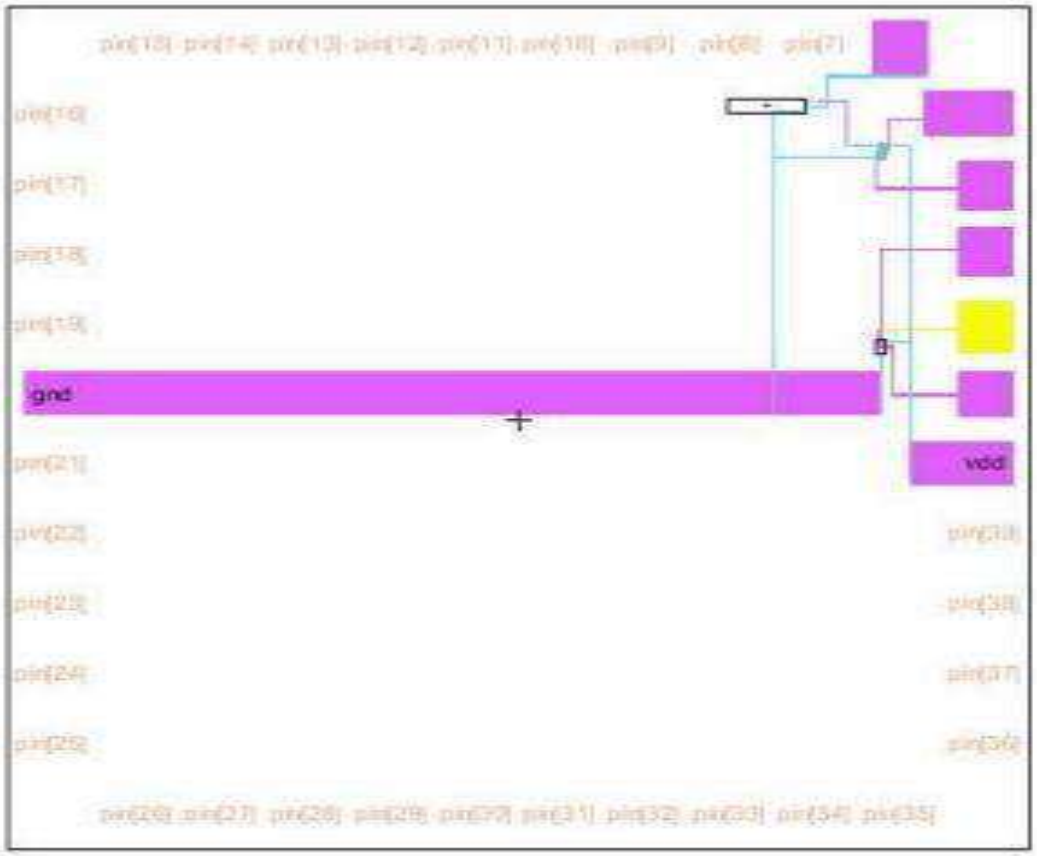
pin[2]
pin[3]
pin[4]
pin[5]
ring_oscillator{sch}
pin[6]
pin[20]
pin[40]
pin[1:40]
padframe



Conclusion / Summary :

Designing of Pad frame was done and Design process is carried using C5 process technology . Additional DRC and LVS checks were done for the overall design.

Lakshmi Narain College of Technology Excellence, Bhopal
Department of Electronics & Communication Engineering

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